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Surface preparation and interfacial stability of high-k dielectrics deposited by atomic layer chemical vapor deposition

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Abstract

The effects of various interface preparations on atomic layer chemical vapor deposition (ALCVD) deposited Al_2O_3 and ZrO_2 dielectrics properties were investigated by X-ray photoelectron spectroscopy (XPS), attenuated total reflection Fourier transform infrared spectroscopy (ATR-FTIR), medium energy ion scattering (MEIS) and transmission electron microscopy (TEM). H-terminated Si, SiO_2 and SiO_xN_y surfaces were used as substrates upon which the dielectric was deposited. Thermal annealing of SiO_2 in NH_3 forms an oxynitride; subsequent deposition of a ZrO_2/Al_2O_3 bi-layer stack resulted in a capacitor structure with an equivalent oxide thickness (EOT) of ~0.8 nm and a leakage current of 3×10^{-4} A/cm^2 at $-1+V_{fb}$. This is in contrast to capacitor structures grown on H-terminated Si where high leakage was found. The growth of additional interfacial SiO_2 during processing, a critical problem in nano-electronic device applications, is temperature dependent with ZrO_2 exhibiting a higher oxygen permeability than Al_2O_3. Use of a polysilicon cap was shown to be effective at blocking oxygen absorption and transport through the high-k dielectrics, with stability up to 1100 °C.

Keywords: Interface; High-k dielectrics; Atomic layer chemical vapor deposition

1. Introduction

In the push to scale gate oxides below 1.0-nm thickness, high leakage currents due to direct electron

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tunneling across SiO_2 are forcing researchers to consider alternative higher dielectric constant (high-k) materials [1,2]. ZrO_2, HfO_2 and Al_2O_3, as well as some metal silicates and aluminates are prime candidates currently under intense investigation [3–6]. Using high-k materials in place of SiO_2 permits an appropriately large capacitance to be obtained while reducing leakage current. Although a SiO_2 interface is not desired in high-k gate stacks because of its low permittivity, a competitive CMOS structure without the Si/SiO_2 interface is yet to be engineered. What is needed is a way to optimize, with atomic layer control, the SiO_2 present at the interface. This involves careful processing, since SiO_2 tends to grow under any conditions in which the system is annealed in an oxygen-containing environment. Furthermore, we and others have found that the surface (which eventually becomes the interface) is critical to both the morphology of the dielectric that is grown [7,8] and the final gate stack electrical characteristics [9]. For instance, heterogenous island growth of high-k materials is observed on H-terminated Si [8], whereas uniform high-k film growth is attained when growing on an OH-terminated Si. Hence, an understanding and control of interfacial oxide growth has become critical to high-k gate dielectric scaling if one is to follow the International Technology Roadmap for Semiconductors (ITRS) requirements. In this work, various surfaces were prepared (ex-situ), high-k films were deposited by atomic layer chemical vapor deposition (ALCVD) [10], and then the physical and electrical properties of the gate stacks were characterized and compared.

2. Experimental

P-type Si substrates (200 mm) experienced surface pre-treatments prior to high-k deposition. Three types of Si surface termination were employed to study the effect on subsequent high-k growth and electrical properties. Si surface termination was achieved via H, N or OH. Preparing a H-terminated Si(100) surface was accomplished by using a 2% HF in H_2O dip for 30 s. The effectiveness of such a treatment was confirmed with X-ray photoelectron spectroscopy (XPS); no oxidized Si was detected in the Si (2p) spectra. Such a H-terminated Si surface is found to be stable for at least 1 h upon air exposure (Fig. 1). N-termination of the Si surface was prepared by annealing a silicon substrate in 10 Torr of NH_3 for 1 min at 560 °C. Subsequent XPS analysis showed that a Si oxynitride signature (rather than pure silicon nitride) was present on the surface, indicative that oxygen was introduced into the film either during annealing or while being transferred in air to the XPS system (Fig. 1). OH-termination on Si was prepared in two ways, either by means of a chemical oxide or rapid thermal oxidation (RTO). The former is achieved by a wet clean process (IMEC clean) [14] resulting in a 0.8-nm thick chemical oxide. The latter is prepared by thermal oxidation in 10 Torr of oxygen where the thickness is primarily controlled by the temperature of oxidation. For instance, a 0.5-nm thick RTO was grown at a temperature of 650 °C for 1 min of oxidation. A hydrophilic surface with OH-termination was generally achieved as characterized by the Si 2p from XPS (Fig. 1).

After surface preparation high-k dielectrics were deposited by ALCVD in an ASM P8200 Polygon Cluster Tool. ALCVD deposition was carried out at 300 °C and ~1 Torr with precursors of water (H_2O), tri-methyl aluminium ($Al(CH_3)_3$) and zirconium tetrachloride ($ZrCl_4$). X-ray photoelectron spectroscopy (XPS) was used to measure the thickness and chemical composition of the Si/high-k interface [11], and the high-k layer thickness was quantified by X-ray fluorescence (XRF). Medium energy ion scattering (MEIS) was used to assess the film stack composition, interfacial oxide

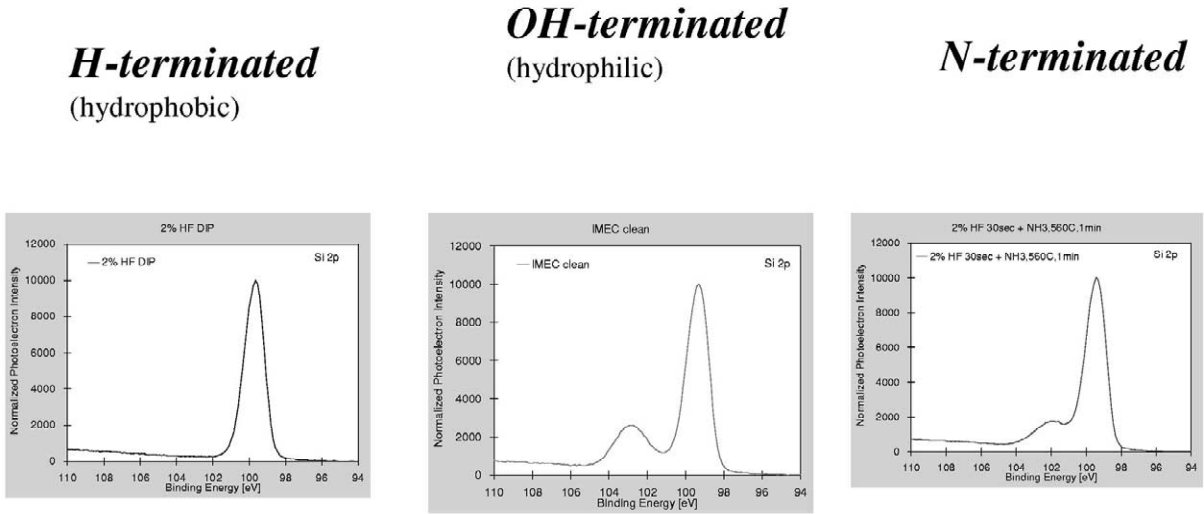

Fig. 1. Si 2p XPS spectra of various interfaces and possible bonding configurations.

thickness and its thermal stability; the details of the MEIS experimental hardware can be found elsewhere [12]. The thickness quantification by XPS was based on the electron mean free path in ZrO_2, Al_2O_3 and SiO_2 of 2.26, 2.7 and 2.96 nm, with thickness calibration of ZrO_2 and Al_2O_3 completed by RBS and ICP-OES, respectively; details of the thickness estimation are described elsewhere [11].

XRF measurements were made using a wavelength dispersive spectrometer (Technos 2400, Philips), relying on Si Kα (109.198 keV), Al Kα (144.915 keV), Zr Lβ1 (126.759 keV) and Zr Lβ2 (126.759 keV) for layer characterization. In order to convert the XRF intensity response into a layer thickness, the theoretical density for both ZrO_2 (5.7 g/cm^3) and Al_2O_3 (3.86 g/cm^3) have been used. Thickness calibration was done similar to XPS [11]. Infrared measurements were performed on a Bruker (IFS-55) Fourier transform infrared (FTIR) spectrometer equipped with an attenuated total reflection (ATR) device [13] and a liquid-N_2-cooled HgCdTe detector. Each spectrum was obtained using the following experimental conditions: p-polarisation, 1000 scans, and 4 cm^{-1} resolution.

3. Results

3.1. Effect of surface preparation on ALCVD growth of Al_2O_3 and ZrO_2

The effect of various surfaces on the Al_2O_3 growth rate is shown in Fig. 2. Film thickness was measured by XRF and XPS. Generally good agreement was obtained between the two techniques, and both were found to be less problematic than ellipsometry where the intrinsic issue of variations of optical constants with thickness remain. On H-terminated Si the initial growth rate of Al_2O_3 is very low, especially for less than 20 ALCVD cycles. The slow initial growth rate arises from the fact that hydrogen effectively passivates the Si surface and thus leads to inhomogeneous island nucleation and

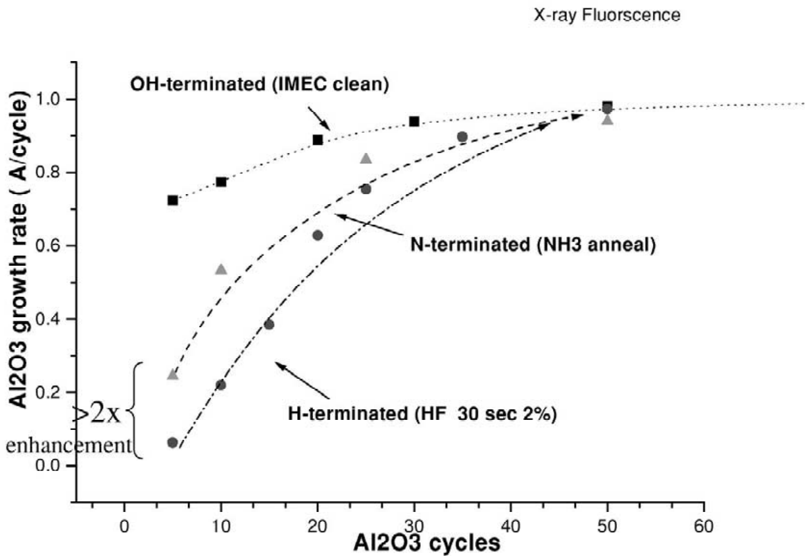

Fig. 2. Effect of interface preparation on ALCVD Al_2O_3 growth kinetics.

a final film that is porous [7,8]. After an incubation time, the growth rate reaches a flat level that is the same for all surfaces. For OH-terminated Si, the initial Al_2O_3 growth is much faster than the H-terminated case, with little inhibition. For the N-terminated Si, the initial growth rate lies between that displayed on the H-terminated and OH-terminated Si surfaces. It is thought that the ligand exchange can potentially occur between the high-k precursor and either OH or NH groups on the NH_3 annealed Si surface. The observed growth inhibition may be due to either a reduced number of surface OH groups as compared to a pure SiO_2 surface or because the ligand exchange rate between the NH groups and the high-k precursor may not be as efficient as for the OH groups. Similar growth rate trends were observed for ALCVD ZrO_2 as a function of these surface preparations.

3.2. Interfacial oxide growth for ALCVD deposited Al_2O_3 and ZrO_2 layers

The next experiment was performed by taking a sample with a given surface preparation, depositing the high-k film by ALCVD and exposing the sample to air. Interfacial oxide growth was checked by XPS. The layer thickness was calculated from peak intensity measurements, according to the thickogram method [15]. As is clearly shown in Fig. 3, growth of an interfacial oxide layer as thin as 0.1 nm is observed. In some cases, an interfacial SiO_2 layer was observed to grow. For example, following ten cycles of Al_2O_3 deposited on a H-terminated Si surface, SiO_2 was found by XPS (as well as MEIS and FTIR, see below) to grow dramatically upon air exposure (Fig. 3). The interfacial SiO_2 thickness grew further during a 500 °C thermal anneal in 10-Torr oxygen (Fig. 4). This is consistent with published reports on the high oxygen transport in CVD-grown, as well as sputter deposited, high-k dielectrics materials [16]. For ALCVD Al_2O_3, the variation of SiO_2 with number of growth cycles is shown in Fig. 5, with and without air exposure effects. The interfacial SiO_2 for as-deposited Al_2O_3 only amounts to ~ 0.1–0.2 nm, whereas the SiO_2 thickness reached ~ 0.5 nm for <20 cycles of Al_2O_3 after air exposure, decreasing to less than 0.2 nm for thicker films. For

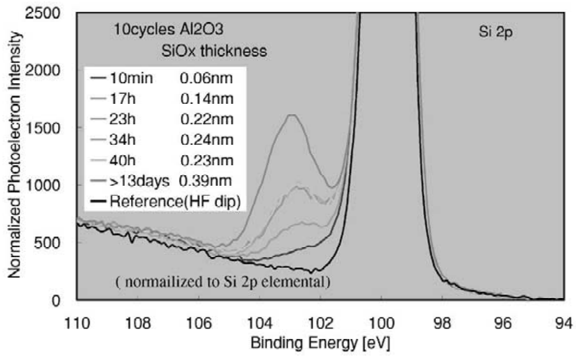

Fig. 3. Effect of air exposure on interfacial oxide growth on ten cycle Al_2O_3 on H-terminated Si.

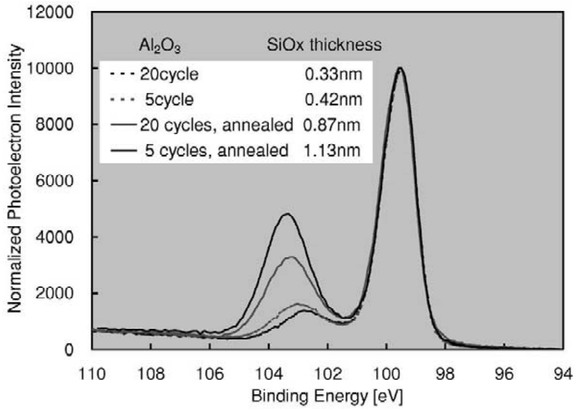

Fig. 4. Effect of thermal anneal in oxygen on five and 20 cycles of Al_2O_3 on H-terminated Si.

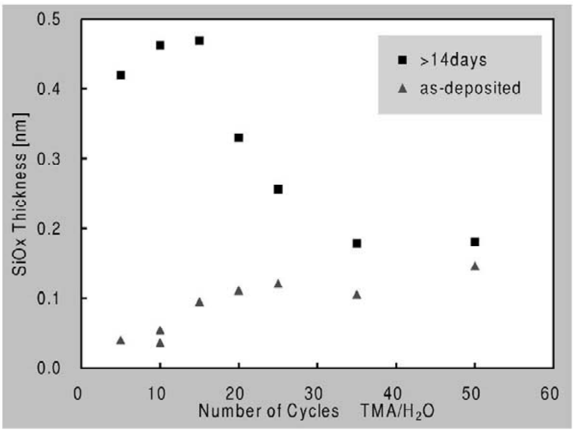

Fig. 5. Interfacial oxide growth of as-deposited and air exposed Al_2O_3 over H-terminated Si.

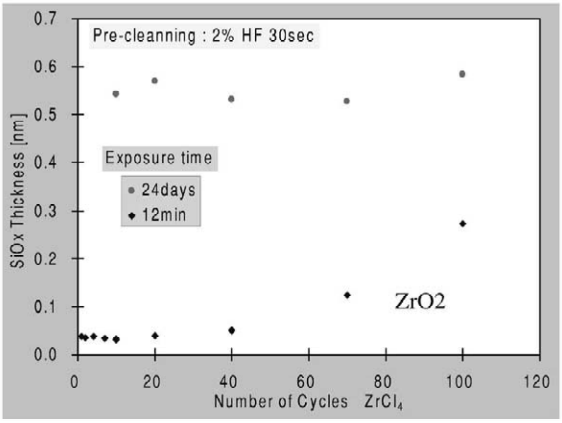

Fig. 6. Interfacial oxide growth of as-deposited and air exposed ZrO_2 over H-terminated Si.

as-deposited ALCVD ZrO_2, the interfacial oxide scales with ZrO_2 thickness (Fig. 6), whereas additional SiO_2 growth stabilizes at ~ 0.5 nm after air exposure. The formation of the SiO_2 interfacial layer, especially for very thin layers, can be due to both the oxidation of exposed Si and to oxidation of Si underneath the Al_2O_3 or ZrO_2 film. By comparing the two high-k materials, it is clear that not only the oxidation of free Si occurs but that diffusion through the layer is also important. To summarize, oxygen permeability through ZrO_2 is generally higher than Al_2O_3. This is consistent with results reported in the literature [16]. Therefore, caution must be taken to prevent prolonged exposure of such high-k materials to an oxidizing environment, especially if the sample is at elevated temperature.

Various high-k gate stack structures were characterized by attenuated total reflection Fourier transform infrared spectroscopy (ATR-FTIR) in an attempt to better understand interface composition and chemistry. From the oxide spectral region of 600–1300 cm^{-1}, the estimated thicknesses of Al_2O_3 and SiO_2 (integrated area of Al–O and Si–O band) versus the number of deposition cycles for the growth of Al_2O_3 on H-terminated Si are shown in Fig. 7 for samples with 1-week air exposure. Interfacial SiO_2 growth was found to decrease with greater Al_2O_3 cycles (i.e. overlayer thickness), indicative of the reduced oxygen transport with increasing dielectric layer thickness. These data show an incubation period at the beginning of the growth of the Al_2O_3 and are consistent with published ALCVD growth kinetics [8], with the growth rate becoming linear after growth inhibition.

The Si–H bonding structure in the 1900–2400 cm^{-1} spectral region for a sample with a dielectric deposited is shown in Fig. 8, with a comparison to a spectrum of a H-terminated Si starting surface (dashed line indicates no dielectric). Three different types of hydrides: SiH, SiH_2 and SiH_3 at 2080, 2110 and 2140 cm^{-1}, respectively, are shown. The Si–H bonding frequency is very sensitive to the environment of the silicon atom; the band shifts with the number of oxygen atoms back-bonded to the silicon (2200 and 2250 cm^{-1} with two and three oxygen back-bonds, respectively). It can be seen that for films that have been exposed to 35 cycles of Al_2O_3, no oxygen back-bonding is measurable, which corresponds to the minimum level of Si–O bonding visible on Fig. 7. This indicates that Al_2O_3 can be grown on silicon essentially without an interfacial oxide. The value of 0.15 nm (from XPS) corresponding to the minimum level of Si–O bonding is likely due to the Si–O–Al linkage. On the other hand, below 35 cycles, oxygen reacts with Si in the substrate during the air exposure of the

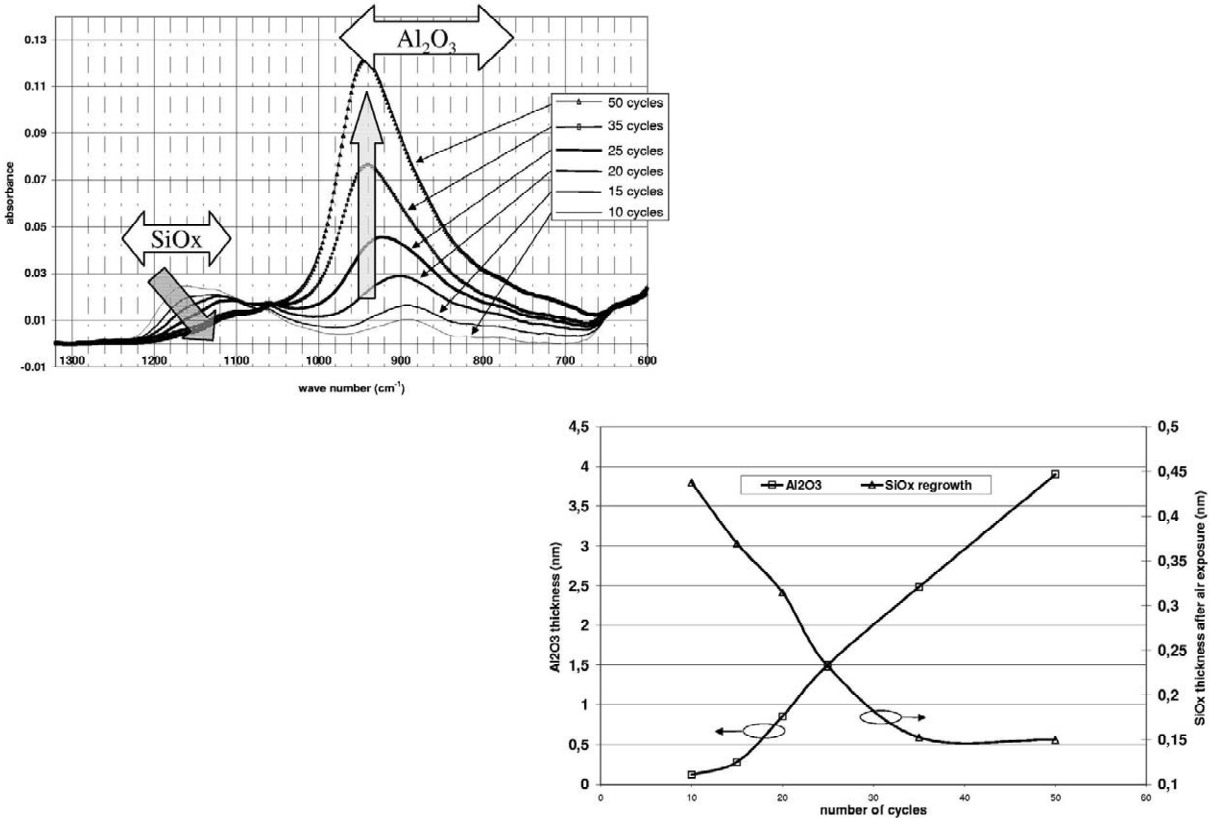

Fig. 7. Oxide modes of FTIR on air exposed Al_2O_3/H-terminated interface.

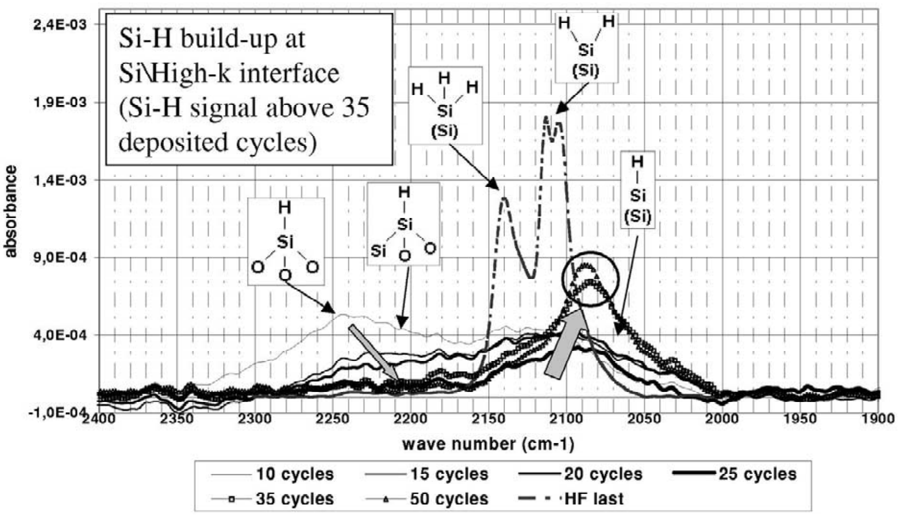

Fig. 8. Si–H stretch region of FTIR on air exposed Al_2O_3/H-terminated interface.

samples. This is due to the fact that below 35 cycles (~2.5 nm), the layer may not be continuous and therefore can not prevent interfacial oxide growth [8]. In summary, the increase of silicon–oxygen back bonding (as measured by XPS and FTIR) with decreasing dielectrics layer thickness is consistent with either (i) rapid oxygen transport through the ultrathin dielectric, or (ii) incomplete coverage of the underlying Si by an inhomogeneous dielectric overlayer.

Regarding the band circled on Fig. 8, it is interesting to note that it is located between the mono-hydride and the di-hydride positions. This indicates that it is related to a different Si–H configuration due to a change of the local environment. The band grows during the deposition of the Al_2O_3 layer and its intensity remains constant after 50 cycles (not shown here). Thus, one reasonable hypothesis is that there is a build up of mono-hydrides when di- and tri-hydrides sites are consumed, perhaps inherent to the interface.

Air exposed Al_2O_3 and ZrO_2 deposited on H-terminated Si were characterized by MEIS. For a nominal 3-nm Al_2O_3 film, areal densities of 1.5×10^{16} atoms/cm^2 for Al + Si imply a negligible amount of interfacial oxide ($< 0.05 \times 10^{15}$ atoms/cm^2), consistent with the <0.1-nm SiO_2 estimated by XPS at this Al_2O_3 thickness (Figs. 5 and 9). For a nominal 3-nm ZrO_2 film, 0.5 nm of interfacial SiO_2 is determined from the ZrO_2 with an areal density of 9.1×10^{15} atoms/cm^2 (Fig. 10), consistent with XPS measurement. Furthermore, a Cl concentration of $\sim 0.3 \times 10^{15}$ atoms/cm^2 was estimated at a depth of 2.5–4 nm, attributed to the use of $ZrCl_4$ precursors in the ALCVD process. In the case of C content in the high-k materials, no significant signal is detected by MEIS, only surface carbon observed from sample handling.

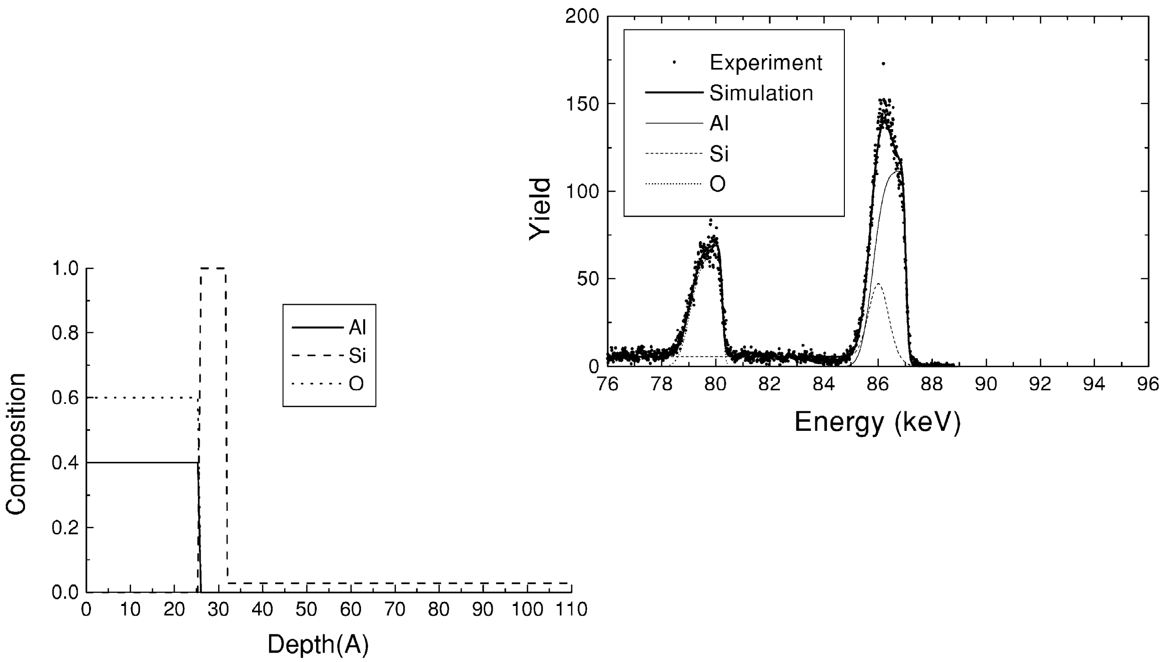

Fig. 9. MEIS spectra of an air exposed Al_2O_3 over H-terminated Si.

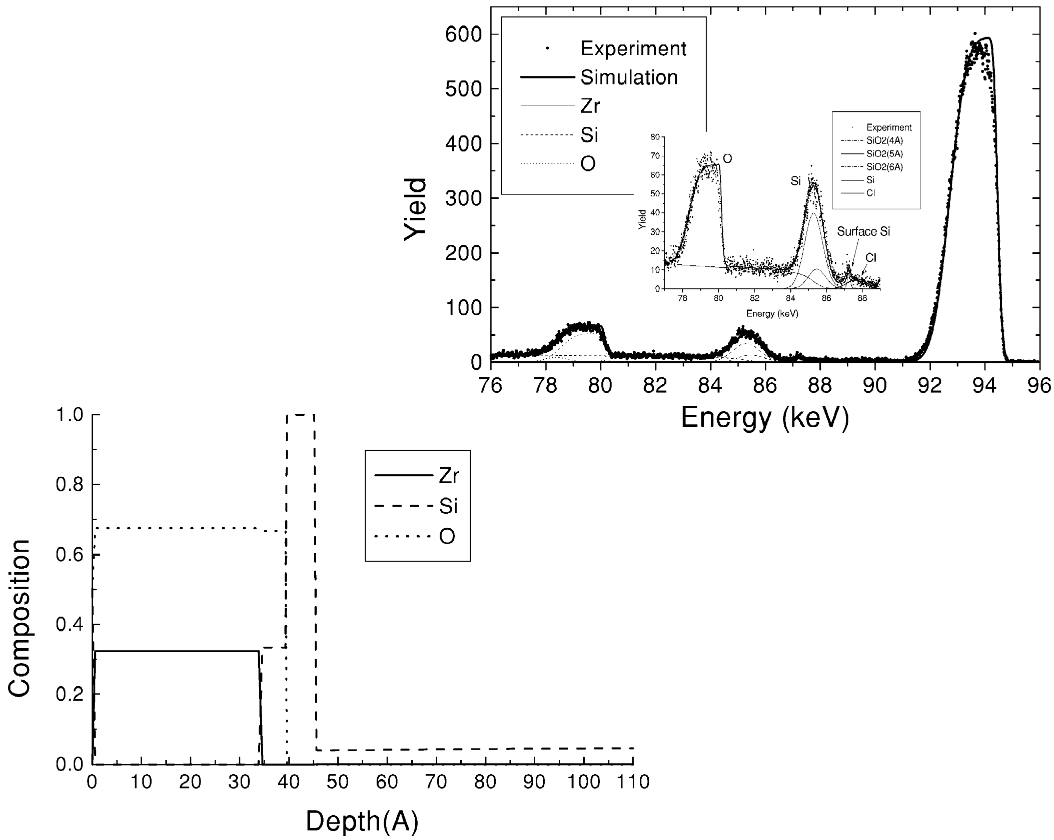

Fig. 10. MEIS spectra of an air exposed ZrO_2 over H-terminated Si.

3.3. Effect of polysilicon capping on interfacial oxide

The effect of a 100-nm polysilicon cap on interfacial oxide growth of an Al_2O_3/H–Si gate stack is shown in Fig. 11, where no additional oxide is formed based on the cross-sectional transmission electron microscopy (TEM) image. The poly-Si cap was deposited in the ASM Polygon Cluster Tool with a RTCVD process after high-k deposition without an air-break. Growth of a SiO_2 interface is suppressed to an annealing temperature as high as 1100 °C in a N_2 ambient with a finite partial pressure of O_2 and H_2O (e.g. 10^{-3} Torr); the oxygen diffusion is apparently blocked by the polysilicon. This result is important in terms of the actual process fabrication as it shows that the total oxygen exposure between high-k deposition and gate electrode deposition must be minimized in order to prevent interfacial oxide growth. It also shows that poly-Si capping of a high-k/Si interface is stable with respect to O in-diffusion, even at 1100 °C. However, the integration of such an in-situ poly-Si cap with a high-k dielectric will need to be evaluated in more detail since the low pressure and relatively high temperature of RTCVD processes generally promotes interfacial reactions between polysilicon and high-k dielectrics such as ZrO_2. The formation of Zr-silicide has been reported to be a major failure mechanism of such poly-Si high-k gate stacks [17,18] at 1000 °C.

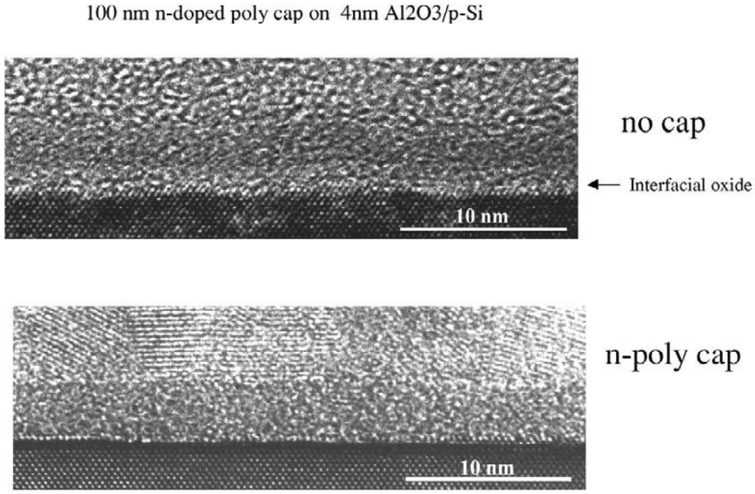

Fig. 11. TEM of a 100-nm polysilicon capped 3-nm Al_2O_3/H-terminated Si and a un-capped 3-nm Al_2O_3/H-terminated Si.

3.4. Effect of surface preparation on electrical characteristics

An example to demonstrate the importance of surface preparation in high-k gate stacks is shown in Fig. 12 where binary stacks of ZrO_2 and Al_2O_3 were deposited on H-terminated and N-terminated p-type Si substrates. Planar capacitors were fabricated with TiN electrodes by wet etch methods followed by a 400 °C forming gas anneal. On the H-terminated interface, a very high leakage was observed primarily due to incomplete film growth of the ZrO_2/Al_2O_3 stack. For the N-terminated surface, with an enhanced growth of Al_2O_3 and ZrO_2 (Fig. 2) a reasonably well-behaved device is reported with an EOT [19] of ~ 0.77 nm and a flatband corrected leakage current of 3×10^{-4} A/cm^2 at $-1 + V_{fb}$.

A second example demonstrating the importance of interface engineering in high-k gate stacks is

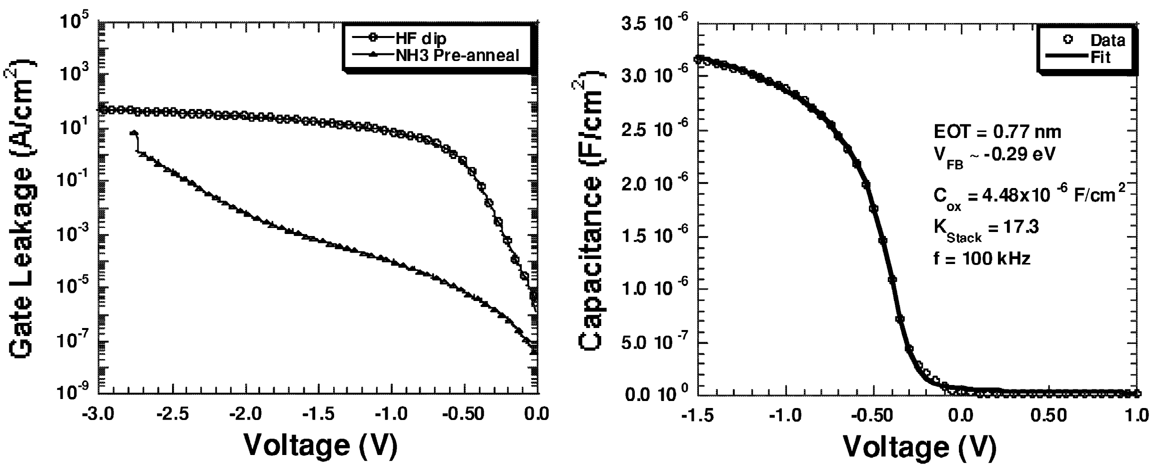

Fig. 12. CV and IV of $TiN/ZrO_2/Al_2O_3$on H-terminated and N-terminated Si.

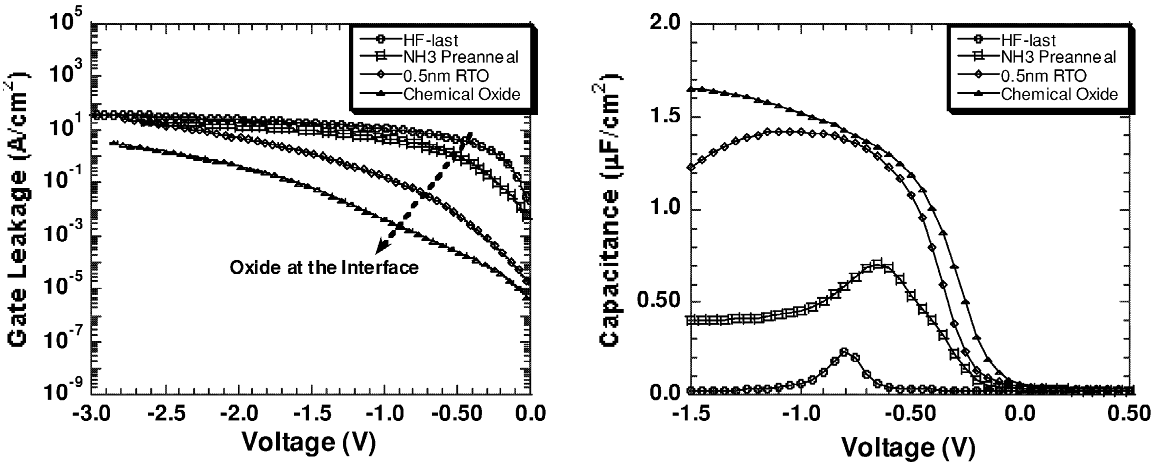

Fig. 13. CV and IV of poly/ZrO_2/$Al_2O_3$with various interface preparations on p-Si.

the effect of poly-Si integration as shown in Fig. 13. Planar capacitors were fabricated from As-doped rapid thermal chemical vapor deposition (RTCVD) poly-Si deposited onto an ALCVD 4-nm ZrO_2/1-nm Al_2O_3 dielectric stack in an ASM cluster tool without air-break. Leakage currents across such poly-Si/high-k devices were found to be modulated by the interface; in particular, very high leakage was observed for deposition on H-terminated surfaces, with leakage being reduced on SiO_2 interfaces (i.e. OH-termination). The Si/high-k interface strongly impacts the subsequent poly-Si interactions with Zr-based high-k dielectrics [20].

In essence, ALCVD growth of high-k materials such as ZrO_2 was significantly enhanced on a OH-terminated Si (almost linear growth curve) versus that on H-terminated Si where strong growth inhibition is present and results in poor quality of high-k crystalline grain-growth and enhanced reactivity with poly electrode. For instance, with a reducing ambient of poly-Si deposition at elevated temperature (e.g. >500 °C), direct epitaxial silicon growth onto the H-terminated Si lattice, through crystallized ZrO_2 layer was shown by cross-section TEM. Formation of Zr-silicide at the interface with the poly electrode was identified by XPS and TEM [20], whereas intact bottom and top interfaces were observed with poly/ZrO_2/Al_2O_3/OH-terminated Si. This is consistent with the enhanced gate leakage mechanism as a function of interfacial oxide shown by both IV and CV in Fig. 13. Hence, surface preparation prior to high-k dielectric deposition is critical to the subsequent poly-Si/high-k integration as it directly influences the high-k film growth morphology and electrical properties.

4. Discussion

The thermal stability and compatibility of high-k gate stacks is important to the successful integration of such materials into conventional CMOS processes. The role of the Si/high-k interface again is critical in this regard as it directly influences the growth morphologies, density and interactions of the high-k with gate electrodes. For example, the thermal stability of an ALCVD 4-nm ZrO_2 stack on H-terminated Si was studied with vacuum annealing using MEIS as shown in Fig. 14. Oxygen loss was observed from the gate stack, attributed to a SiO desorption and Zr-silicide

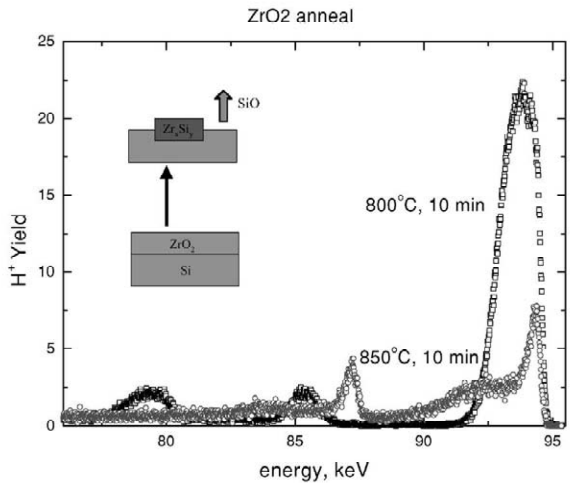

Fig. 14. MEIS spectra of a thermally annealed ZrO_2 over H-terminated Si.

formation mechanism for reducing anneals at $T > 850\,°C$. For ZrO_2 stacks deposited on an OH-terminated interface, the thermal stability is much improved, attributed to more uniform and dense high-k film. Furthermore, the thermal integrity of high-k stacks and their interfaces are highly sensitive to process variables such as anneal ambient (e.g. oxygen) from various gas–surface interaction mechanisms [21] and thermal processing history [22], and the role of surface preparation before high-k deposition directly influences such gas–surface interactions.

For the N-terminated interface which after dielectric and electrode deposition shows low EOT and leakage currents (by us as well as others [23]), there are inherent issues of carrier mobility degradation [24]. The mechanism of such degradation is currently under investigation and one way to improve mobility in the case of the nitride interface is to incorporate oxygen species (e.g. oxynitride) by thermal anneal in an oxidative ambient. This in turn creates an interface more SiO_2-like in nature as is necessary to maintain reasonable mobility [25]. The speculation here is that a SiO_2-like interface, (generally present in high-k gate stack preparation), with minimum thickness to be determined, will behave as a Si–SiO_2 interface where reasonable mobility can be achieved.

To achieve scaling of high-k gate stacks to the sub-1 nm EOT regime, the ability to control interfacial oxide growth is a key factor. The OH-terminated Si surface was shown in the current work to be better than the H-terminated surface for subsequent high-k growth as well as poly-Si integration. However, the thickness of the chemical or rapid thermal oxide interface generally is too large and remains a serious challenge for scaling. One remedy to this scenario is that the interfacial oxide may undergo some densification or reduction after high temperature processing. For example it has been reported that a chemical oxide from an SC1/SC2 clean with an initial thickness of 1-nm densifies to ~0.6 nm after a full CMOS process [26]. Understanding the densification process of such SiO_2 interfaces is a key area of current research. Furthermore, the growth of the interfacial oxide for various exposures and temperature cycles also needs to be carefully monitored during processing, including the total exposure to oxidizing gases.

5. Conclusions

Surface preparation and interface stability is a critical step that must be resolved to enable the implementation of high-k dielectrics for sub-0.1 μm gate stacks. The growth of ALCVD dielectrics is strongly inhibited by H-terminated Si surfaces whereas almost no inhibition is observed on OH-terminated surfaces. For H-terminated Si, high SiO_2 interfacial growth was observed for ALCVD Al_2O_3 and ZrO_2 dielectrics. Gate leakage current, CV quality and poly-Si integration of high-k devices were found to be strongly modulated by the surface preparation prior to high-k deposition.

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