High-Mobility Stable 4H-SiC MOSFETs Using a Thin PSG Interfacial Passivation Layer

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***Abstract*—Phosphorous from P_2O_5 is more effective than nitrogen for passivating the 4H-SiC/SiO_2 interface. The peak value of the field-effect mobility for 4H-SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) after phosphorus passivation is approximately 80 $cm^2/V \cdot s$. However, P_2O_5 converts the SiO_2 layer to phosphosilicate glass (PSG)—a polar material that introduces voltage instabilities which negate the benefits of lower interface trap density and higher mobility. We report a significant improvement in voltage stability with mobilities as high as 72 $cm^2/V \cdot s$ for MOSFETs fabricated with a thin PSG gate layer ($\sim$10 nm) capped with a deposited oxide.**

***Index Terms*—MOSFET, silicon carbide, stability, thin phosphosilicate glass (PSG).**

I. Introduction

SILICON carbide MOSFETs have historically been plagued by very low channel electron mobility that results from a high density of interface traps at the SiC/SiO_2 interface. Significant progress has been made with respect to interface passivation over the last decade, specifically with the advent of nitric oxide postoxidation annealing [1], [2] which provides an acceptable channel mobility of around 35 $cm^2/V \cdot s$. This process has been a key factor in the recent commercialization of SiC MOSFETs. However, the channel resistance in state-of-the-art 4H-SiC power MOSFETs still contributes to about half the total conduction loss [3]. Therefore, higher channel mobility is crucial for next-generation devices. The channel resistance is inversely proportional to the inversion channel carrier mobility which is determined by the quality of the oxide–semiconductor interface [4], [5]. As mentioned, the peak value of the inversion channel mobility with stable threshold voltage (V_{TH}) is currently around 35 $cm^2/V \cdot s$, obtained with NO passivation. This value is only 4% of the bulk mobility of 4H-SiC ($\sim$800–1000 $cm^2/V \cdot s$) [6]. Reports indicate that phosphorus passivation (P-passivation) is more effective than NO passivation, providing peak mobilities of 80–90 $cm^2/V \cdot s$ [7], [8] for devices fabricated on the conventional (0001) Si-face. The peak mobilities are even higher, about 125 $cm^2/V \cdot s$ for the $(11\bar{2}0)$ a-face, as reported in a recent paper [9].

However, after P-passivation, the oxide is no longer SiO_2 but rather is transformed to phosphosilicate glass (PSG). The polar characteristics of PSG cause threshold voltage instabilities [8], [10]. Herein, we describe a process of forming a thin PSG interfacial layer ($\sim$10 nm) capped by a thick SiO_2 layer ($\sim$35 nm) that provides much improved voltage stability and high mobility ($\sim$70 $cm^2/V \cdot s$) for MOSFETs fabricated on the (0001) Si-face of 4H-SiC.

II. Experiment

The material for device fabrication was provided by Dow Corning and Cree, Inc. MOS capacitors were fabricated using 8° off-axis (0001) Si-face n-4H-SiC wafers with 5-μm n-epilayers doped with nitrogen at 8.3×10^{15} cm^{-3}. A thin thermal oxide (6–8 nm) was grown at 1150 °C and later passivated (2 h at 1000 °C) in a phosphorous planar diffusion source (PDS) furnace [8] to produce a PSG layer of around 10-nm thickness. All samples were capped with an oxide layer ($\sim$35 nm) deposited by cracking tetraethyl orthosilicate (TEOS) at 650 °C and 0.6 torr in a low-pressure chemical vapor deposition (LPCVD) system. The TEOS oxide was annealed in nitrogen (2 h at 850 °C) immediately after deposition. Molybdenum was sputter deposited to form gate contacts, and broad-area silver-paste backside contacts were applied after backside oxide removal. Interface trap densities were determined from simultaneous high–low frequency (1 MHz/quasi-static) capacitance–voltage (C–V) measurements performed at room temperature.

Planar MOSFETs with gate lengths of 150 μm and gate widths of 290 μm were fabricated on aluminum-doped (8×10^{15} cm^{-3}) 4° off-axis 5-μm p-epilayers grown on n^- substrates. Box nitrogen profiles (6×10^{19} cm^{-3}) with n^+/p junction depths of around 400 nm were implanted to form the FET source/drain regions. The implanted surfaces were protected with carbon caps during activation anneals in Ar (30 min at 1550 °C). The cap layers were later removed using an oxygen plasma (sample temperature $\sim$150 °C–250 °C). A 20-nm sacrificial oxide was grown thermally and removed with buffered HF prior to the thermal growth of the 6–8-nm gate oxide layer. As mentioned earlier, the 2-h P-passivation anneal produced a PSG layer of about-10-nm thickness that was capped with the TEOS LPCVD-deposited oxide. Source/drain and gate contacts were formed by sputtering Ni and Mo, respectively, with an ohmic contact anneal (30 s at 950 °C in Ar) immediately afterward.

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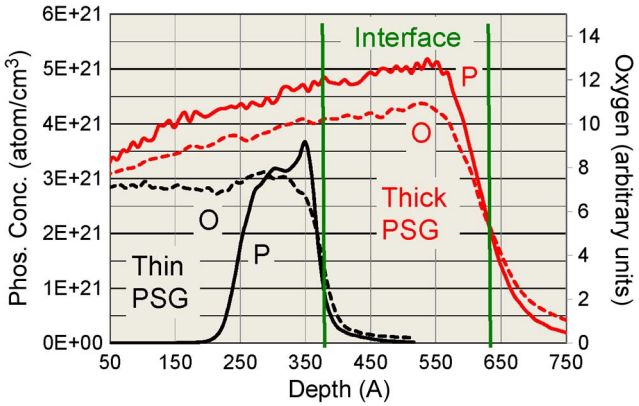

Fig. 1. SIMS profiles for PSG MOSFETs. The phosphorous concentrations are accurate only in the oxide and PSG layers.

III. Results and Discussion

Secondary ion mass spectrometry (SIMS) profiles are shown in Fig. 1 for a thin PSG MOSFET that was also used for mobility measurements that will be discussed later in this section. For comparison, profiles from [11] for a thick PSG MOSFET are also included. Both MOSFETs had similar PDS anneals (2 h at 1000 °C); however, a different PDS was used for the thin PSG devices (capacitors and MOSFETs). The SiC/SiO_2 interfaces are located at depths (∼38 and 63 nm) where the oxygen signals drop to half their peak values. The dielectric layer thicknesses for thin PSG MOS capacitors from several samples annealed with the MOSFET sample ranged from 42 to 49 nm. The effective oxide thicknesses were calculated using the accumulation capacitance and the dielectric constant of pure SiO_2, and thickness variations likely indicate nonuniform phosphorous uptake from the P_2O_5 ambient during the PDS anneal.

The atomic concentrations for the phosphorous profiles in Fig. 1 are approximately accurate on the PSG side of the interface. The profile for thin PSG phosphorous is slightly asymmetric, with a somewhat more diffused profile appearing on the glass side of the interface. Possibly, phosphorous diffuses from the PSG layer into the oxide cap layer during the 2-h 850 °C densification anneal that follows the TEOS oxide deposition. At the thin PSG–SiC interface, the phosphorous concentration is significantly less than the phosphorous concentration at the thick PSG–SiC interface. These concentrations are consistent with the results of the interface trap density measurements that are discussed in the following paragraph. Other features of the thin PSG profile (e.g., peak near the interface and the tail extending into the SiC) require further study. These features may be due to SIMS artifacts, or they may represent changes associated with the processing.

The results of the C–V measurements for n-4H-SiC MOS capacitors are shown in Fig. 2(a). The interface trap density $(D_{\rm it})$ at 0.2 eV below the SiC conduction band edge for the thin PSG process is approximately two times lower than that of NO but somewhat higher than that of thick PSG. The mobility results for lateral n-channel 4H-SiC MOSFETs are shown in Fig. 2(b). These results are consistent with the measured trap densities. A previous study with NO of the effect of variable nitrogen content has also shown a monotonic dependence on increasing mobility with decreasing interface trap density [11]. The thin PSG MOSFET peak mobility of 72 $\rm cm^2/V \cdot s$ is approximately two times higher compared to that of NO but

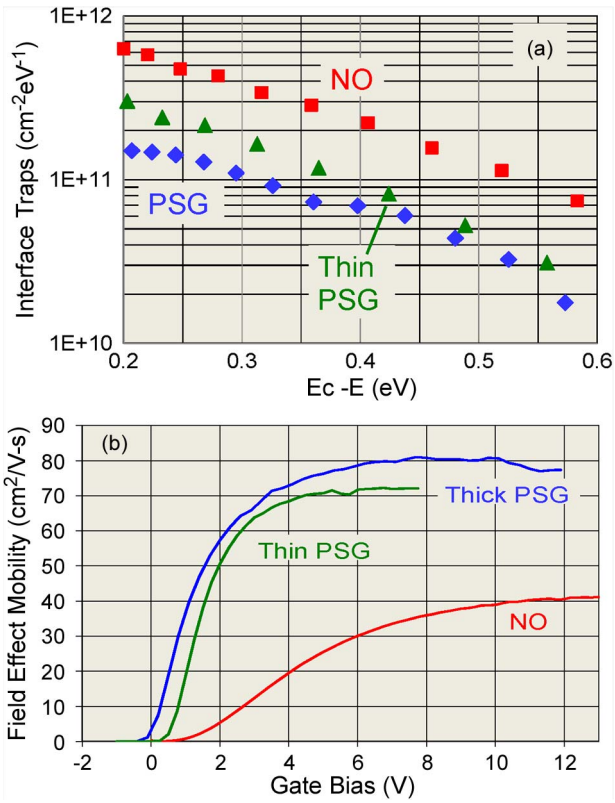

Fig. 2. (a) Interface trap densities for 4H-SiC MOS capacitors. (b) Channel mobilities for passivated 4H-SiC MOSFETs.

is slightly lower compared to that of the thick PSG MOSFET (fully converted gate layer). However, the thick PSG FET is plagued by threshold voltage instability.

The results of positive and negative bias–temperature stress (BTS) measurements for MOS capacitors are shown in Fig. 3(a). The flatband voltage was measured before and after BTS for a different capacitor for each of the BTS times indicated.

a) Positive BTS (solid symbols): The positive shift in flatband voltage $(\Delta V_{\rm FB})$ for the thin PSG capacitors is due to electron trapping in oxide border states—a well-known phenomenon in NO devices [12]. Compared to that for the thick PSG capacitors, $V_{\rm FB}$ is more stable for the thin PSG capacitors, and the shifts are positive, whereas negative shifts are observed for the thick PSG capacitors. These results suggest that positive polarization charge at the interface dominates electron trapping in the thick PSG capacitors but that this charge is either absent or present in significantly lower concentrations in the thin PSG capacitors. The maximum flatband voltage shift measured for the thin PSG capacitors is 1.3 V.

b) Negative BTS (open symbols): The positive flatband voltage shift for the thick PSG n-type capacitor is consistent with negative polarization charge at the interface. The oxide field is smaller for negative gate bias, and the measured shift is much smaller compared to the shift observed for positive BTS. A shift of similar magnitude but opposite sign is observed for the thin PSG capacitors. This shift is not consistent with negative polarization charge at the interface. These observations led us to focus on positive BTS measurements since our primary goal was to evaluate the polarization charge mitigation effect using the thin PSG approach. A more extensive study of negative bias-temperature stressing will be undertaken when optimized thin PSG fabrication procedures are developed.

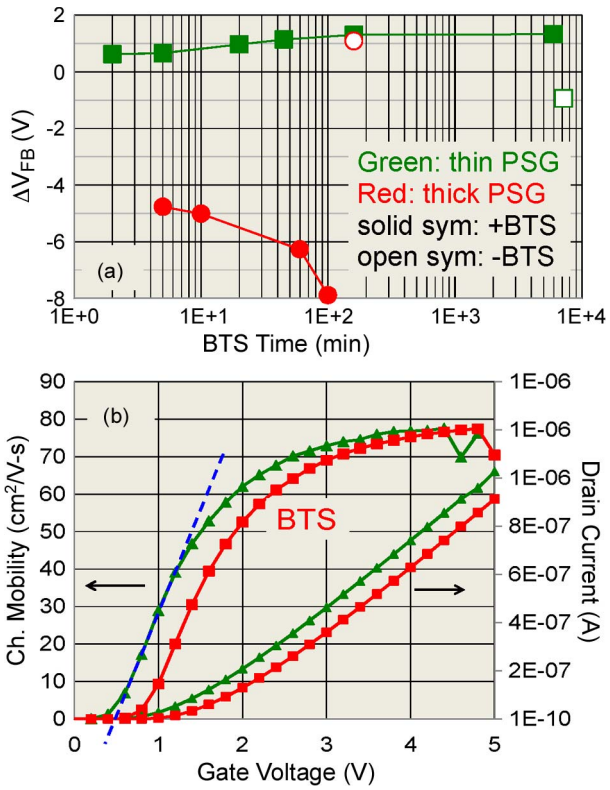

Fig. 3. (a) BTS-induced flatband voltage shifts ($\Delta V_{\rm FB}$) for PSG MOS capacitors. (b) Effects of positive BTS on thin PSG MOSFET threshold voltage and channel mobility. *BTS conditions*: 150 °C, $+V_g$ ($E_{\rm ox} = 1.5$ MV/cm), and $-1.5V_g$ for n-MOS capacitors; 150 °C, 8 h, and $+V_g$ used for thin PSG MOSFETs.

The mobility curves for a thin PSG MOSFET before and after 8 h of positive BTS are shown in Fig. 3(b). There is only a small right shift in the mobility curve with no change in the peak value of the mobility. The small shift of ~0.3 V is further evidence of improved stability in the thin PSG device due to a reduction in polarization charge when the thickness of the interfacial PSG layer is reduced. After passivation, this layer thickness is around 10 nm for the thin PSG devices compared to 70 nm for the thick PSG MOSFET.

The oxide fields during positive stress are similar for the FET and the companion thin PSG MOS capacitors. However, the threshold voltage shift measured for the MOSFET is less than the flatband voltage shift measured for the capacitors. This difference is likely the result of several factors: 1) greater relaxation of trapped electrons from the near-interfacial oxide in the FET due to the presence of holes that are majority carriers in the semiconductor; 2) imprecise determination of the FET threshold voltage using the simple linear extrapolation method; and 3) statistical variations in the flatband voltages that result from using a different capacitor for each BTS time.

The authors in [10] identify short- and long-term polarization effects in PSG oxides (time scales on the order of minutes and hundreds of hours, respectively). They suggest that the MOS capacitor flatband voltage shift due to polarization charge is proportional to the ratio of *PSG layer thickness* to *non-PSG oxide layer thickness*

$$\Delta V_{\rm FB} = \frac{Q_p}{C_g} = \frac{Q_p t_g}{\varepsilon_o K_g} = \left(\frac{t_g}{t_o}\right) \frac{K_o X_p V_p}{K_g[K_g + X_p + K_o t_g/t_o]}$$

where Q_p is the polarization charge, C_g is the PSG layer capacitance, t_g is the PSG layer thickness, t_o is the oxide layer thickness, K_g is the PSG dielectric constant, K_o is the oxide dielectric constant, ε_o is the oxide permittivity, X_p is the PSG polarizability, and V_p is the applied voltage during BTS.

For a given bias voltage, $\Delta V_{\rm FB}$ decreases as the ratio t_g/t_o decreases. By reducing the thickness of the PSG layer, the short-term stability of the MOSFET can be improved significantly. There is likely a minimum PSG layer thickness that will preserve the trap passivation effect of phosphorous. We used a 10-nm PSG layer, but we have not determined whether this thickness might be reduced further for even better stability while preserving the trap passivation effect.

IV. Conclusion

We have shown that, by reducing the thickness of an interfacial PSG gate dielectric layer, the threshold voltage stability of phosphorous-passivated 4H-SiC MOSFETs can be improved significantly without sacrificing the beneficial effect of P-passivation for lower interface trap density and higher effective channel mobility. Our results are applicable for the short-term polarization effects described in [10]. Additional work is underway to further optimize the thin PSG process and to fully investigate the long-term polarization effects, including temperature dependence, identified in [10].

References

[1] G. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, O. W. Holland, L. C. Feldman, M. K. Das, and J. W. Palmour, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," *Electron Device Lett.*, vol. 22, no. 4, pp. 176–178, Apr. 2001.

[2] P. Jamet, S. Dimitrijev, and P. Tanner, "Effects of nitridation in gate oxides grown on 4H-SiC," *J. Appl. Phys.*, vol. 90, no. 10, pp. 5058–5063, Nov. 2001.

[3] L. Cheng, A. K. Agarwal, S. Dhar, S.-H. Ryu, and J. Palmour, "Static performance of 20 A, 1200 V 4H-SiC power MOSFETs at temperatures of −187 °C to 300 °C," *J. Electron. Mater.*, vol. 41, no. 5, pp. 910–914, May 2012.

[4] R. Schorner, P. Federichs, D. Peters, and D. Stephani, "Significantly improved performance of MOSFETs on silicon carbide using the 15R-SiC polytype," *IEEE Electron Device Lett.*, vol. 20, no. 5, pp. 241–244, May 1999.

[5] S. Dhar, S. Wang, J. R. Williams, S. T. Pantelides, and L. C. Feldman, "Interface passivation for silicon dioxide layers on silicon carbide," *MRS Bull.*, vol. 30, no. 4, pp. 288–292, Apr. 2005.

[6] J. B. Casady and R. W. Johnson, "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid State Electron.*, vol. 39, no. 10, pp. 1409–1422, Oct. 1996.

[7] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, and T. Fuyuki, "Improved inversion channel mobility in 4H-SiC MOSFETs on Si face utilizing phosphorus-doped gate oxide," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 710–712, Jul. 2010.

[8] Y. K. Sharma, A. Claude, T. Smith, X. Shen, S. T. Pantelides, X. Zhu, J. Rozen, Y. Xu, E. Garfunkel, and J. R. Williams, "Phosphorous passivation of the $SiO_2/4H$-SiC interface," *Solid State Electron.*, vol. 68, pp. 103–107, Feb. 2012.

[9] G. Liu, A. C. Ahyi, Y. Xu, T. Isaacs-Smith, Y. K. Sharma, J. R. Williams, L. C. Feldman, and S. Dhar, "Enhanced inversion mobility on 4H-SiC $(11\bar{2}0)$ using phosphorus and nitrogen interface passivation," *IEEE Electron. Dev. Lett.*, vol. 34, no. 2, pp. 181–183, Feb. 2013.

[10] E. H. Snow and B. E. Deal, "Polarization phenomena and other properties of phosphosilicate glass films on silicon," *J. Electrochem. Soc.*, vol. 113, no. 3, pp. 263–269, Mar. 1966.

[11] J. Rozen, A. C. Ahyi, X. Zhu, J. R. Williams, and L. C. Feldman, "Scaling between channel mobility and interface state density in SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3808–3811, Nov. 2011.

[12] A. J. Lelis, D. B. Habersat, R. Green, and N. Goldsman, "Dependence of SiC MOSFET threshold-voltage instability," *Silicon Carbide Rel. Mater.*, vol. 600–603, pp. 807–810, 2009.