APPLIED PHYSICS REVIEWS

Ultrathin (<4 nm) SiO_2 and Si–O–N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits

M. L. Green[a)]
Agere Systems, Murray Hill, New Jersey 07974

E. P. Gusev
IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598

R. Degraeve
IMEC, Leuven 3001, Belgium

E. L. Garfunkel
Rutgers University, Piscataway, New Jersey 08854

(Received 1 March 2001; accepted for publication 21 May 2001)

The outstanding properties of SiO_2, which include high resistivity, excellent dielectric strength, a large band gap, a high melting point, and a native, low defect density interface with Si, are in large part responsible for enabling the microelectronics revolution. The Si/SiO_2 interface, which forms the heart of the modern metal–oxide–semiconductor field effect transistor, the building block of the integrated circuit, is arguably the worlds most economically and technologically important materials interface. This article summarizes recent progress and current scientific understanding of ultrathin (<4 nm) SiO_2 and Si–O–N (silicon oxynitride) gate dielectrics on Si based devices. We will emphasize an understanding of the limits of these gate dielectrics, i.e., how their continuously shrinking thickness, dictated by integrated circuit device scaling, results in physical and electrical property changes that impose limits on their usefulness. We observe, in conclusion, that although Si microelectronic devices will be manufactured with SiO_2 and Si–O–N for the foreseeable future, continued scaling of integrated circuit devices, essentially the continued adherence to Moore's law, will necessitate the introduction of an alternate gate dielectric once the SiO_2 gate dielectric thickness approaches ~1.2 nm. It is hoped that this article will prove useful to members of the silicon microelectronics community, newcomers to the gate dielectrics field, practitioners in allied fields, and graduate students. Parts of this article have been adapted from earlier articles by the authors [L. Feldman, E. P. Gusev, and E. Garfunkel, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 1 [Ref. 1]; E. P. Gusev, H. C. Lu, E. Garfunkel, T. Gustafsson, and M. Green, IBM J. Res. Dev. **43**, 265 (1999) [Ref. 2]; R. Degraeve, B. Kaczer, and G. Groeseneken, Microelectron. Reliab. **39**, 1445 (1999) [Ref. 3]. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1385803]

TABLE OF CONTENTS

I. INTRODUCTION AND OVERVIEW. 2058
A. SiO_2 enabled the microelectronics revolution... 2058
B. Fundamental limits of SiO_2: Is the end in sight?. 2060
II. PHYSICAL CHARACTERIZATION METHODS FOR ULTRATHIN DIELECTRICS. 2062
A. Optical methods. 2062
B. X-ray based methods. 2065
C. Ion beam analysis. 2067
D. Electron microscopy. 2072
E. Scanning probe microscopy. 2073
III. ELECTRICAL CHARACTERIZATION METHODS AND PROPERTIES. 2074
A. Characterization methods. 2075
1. $C-V$ measurements. 2075
2. Gate tunnel current. 2076
3. Charge pumping. 2077
B. Oxide degradation during electrical stress. 2078
1. Interface trap creation. 2078
2. Oxide charge trapping. 2078
3. Hole fluence. 2078
4. Neutral electron trap generation. 2079
5. Stress-induced leakage current. 2080
6. Discussion of trap generation mechanisms.. 2081

[a)]Electronic mail:mlg@agere.com

 © 2001 American Institute of Physics

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

C. Oxide breakdown. 2082
1. Breakdown modeling. 2082
2. Soft breakdown. 2083
3. Breakdown acceleration models. 2084
4. Temperature dependence of breakdown. . . . 2085
5. Oxide reliability predictions. 2086
IV. FABRICATION TECHNIQUES FOR ULTRATHIN SILICON OXIDE AND OXYNITRIDES. 2086
A. Surface preparation. 2086
B. Fabrication of ultrathin oxide and oxynitrides. . 2086
1. Thermal oxidation and oxynitridation. 2086
2. Chemical deposition. 2088
3. Physical deposition. 2090
C. Postoxidation processing and annealing. 2090
D. Hydrogen/deuterium processing. 2091
V. THE Si/SiO_2 SYSTEM. 2093
A. The initial stages of oxygen interaction with silicon surfaces. 2093
1. The passive oxidation regime. 2094
2. The active oxidation regime. 2098
3. The transition regime. 2099
B. Growth mechanisms of ultrathin oxides, beyond the Deal–Grove model. 2100
VI. THE Si/SiO_xN_y SYSTEM. 2104
A. Oxynitride properties. 2104
1. Thermodynamics of the Si–O–N system. . . 2104
2. Physical properties. 2105
3. Diffusion barrier properties of oxynitride layers. 2105
B. Oxynitridation processes. 2106
1. NO processing. 2106
2. N_2O processing. 2107
a. Gas phase N_2O decomposition at high temperatures. 2107
b. N incorporation and removal during N_2O oxynitridation. 2108
3. Nitridation in NH_3. 2109
4. Nitridation in N_2. 2109
VII. THE POST-SiO_2 ERA: ALTERNATE GATE DIELECTRICS. 2109
A. Si_3N_4. 2110
B. Alternate (higher) dielectric constant materials. 2110

TABLE I. Selected properties of SiO_2 gate dielectric layers.

Native to silicon (SiO_2 is the only stable oxide phase on Si)
Low interfacial (Si/SiO_2) defect density ($\sim 10^{10}\ eV^{-1}\ cm^{-2}$, after H_2 passivation)
Melting point=1713 °C
Energy gap=9 eV
Resistivity $\sim 10^{15}\ \Omega$ cm
Dielectric strength $\sim 1\times 10^7$ V/cm
Dielectric constant=3.9

I. INTRODUCTION AND OVERVIEW

A. SiO_2 enabled the microelectronics revolution

Nature has endowed the silicon microelectronics industry with a wonderful material, SiO_2, as is shown in Table I. SiO_2 is native to Si, and with it forms a low defect density interface. It also has high resistivity, excellent dielectric strength, a large band gap, and a high melting point. These properties of SiO_2 are in large part responsible for enabling the microelectronics revolution. Indeed, other semiconductors such as Ge or GaAs were not selected as the semiconducting material of choice, mainly due to their lack of a stable native oxide and a low defect density interface. The metal–oxide–semiconductor field effect transistor (MOSFET), Fig. 1, is the building block of the integrated circuit. The Si/SiO_2 interface, which forms the heart of the MOSFET gate structure, is arguably the worlds most economically and technologically important materials interface. The ease of fabrication of SiO_2 gate dielectrics and the well passivated Si/SiO_2 interface that results have made this possible. SiO_2 has been and continues to be the gate dielectric par excellence for the MOSFET. Figure 2 is a transmission electron photomicrograph of an actual submicron MOSFET, showing the SiO_2 gate dielectric as well as the Si/SiO_2 interface.

In spite of its many attributes, however, SiO_2 suffers from a relatively low dielectric constant (κ=dielectric constant, or permittivity, relative to air=3.9). Since high gate dielectric capacitance is necessary to produce the required drive currents for submicron devices,[1,4] and further since capacitance is inversely proportional to gate dielectric thickness, the SiO_2 layers have of necessity been scaled to ever thinner dimensions, as is shown in Fig. 3. This gives rise to a number of problems, including impurity penetration through the SiO_2, enhanced scattering of carriers in the

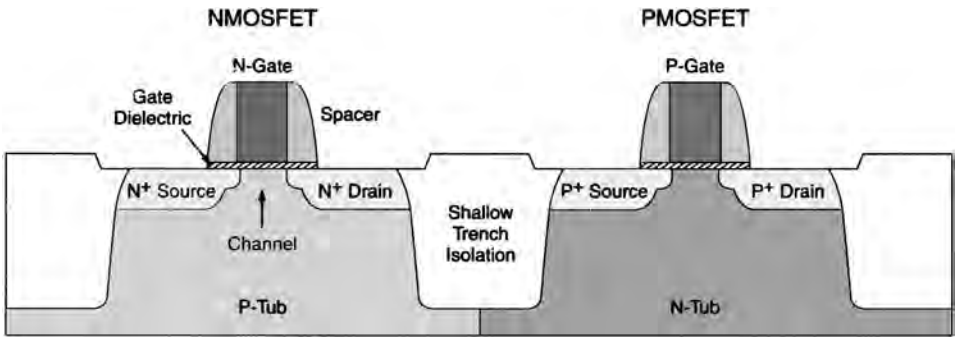


FIG. 1. Schematic illustration of a submicron (channel length) CMOSFET (complementary metal–oxide–semiconductor field effect transistor) (courtesy of C. P. Chang, Agere Systems).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

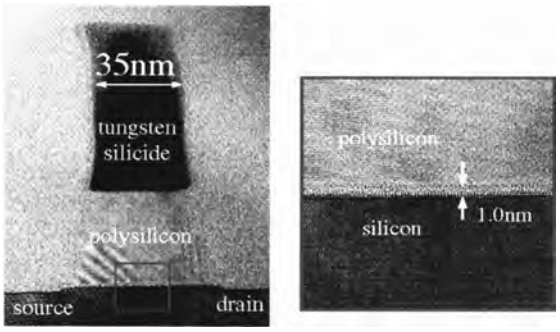


FIG. 2. Cross-section transmission electron photomicrographs of a 35 nm (channel length) transistor, and a detailed view of its 1.0 nm SiO_2 gate dielectric and Si/SiO_2 interface [from Timp *et al.* (Ref. 15)].

channel, possible reliability degradation, high gate leakage current, and the need to grow ultrathin and uniform SiO_2 layers.

This article summarizes recent progress and current scientific understanding of ultrathin (<4 nm) SiO_2 and Si–O–N gate dielectrics on silicon based devices. (Si–O–N will refer to oxynitride dielectrics for which $N/(N+O) \leqslant 0.5$, and most often much less than that.) We will emphasize an understanding of the limits of these gate dielectrics, i.e., how their continuously shrinking thickness, dictated by integrated circuit device scaling, results in physical and electrical property changes that impose limits on their usefulness. We will also discuss the near-future need for alternate gate dielectric materials such as Si_3N_4 and other metal oxides and nitrides, known as "high κ" materials.

In a continuous drive to increase integrated circuit performance through shrinkage of the circuit elements, the dimensions of MOSFETs and other devices have been scaled since the advent of integrated circuits about 40 years ago, according to a trend known as Moore's law.[5–8] Moore's law describes the exponential growth of chip complexity due to decreasing minimum feature size, accompanied by concurrent improvements in circuit speed, memory capacity, and cost per bit. SiO_2 gate dielectrics have decreased in thickness

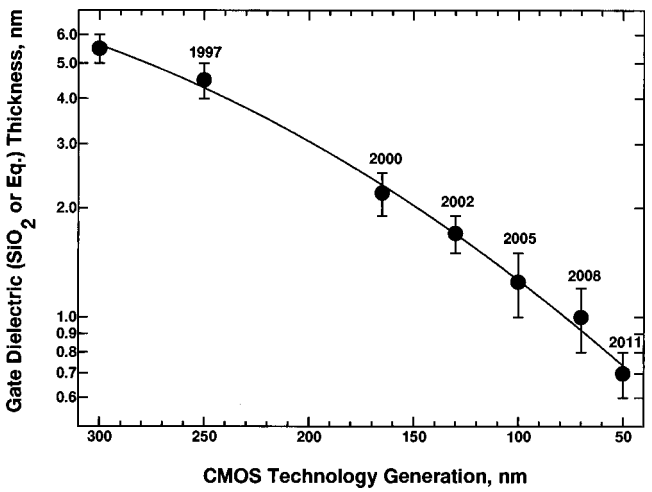


FIG. 3. Decrease in gate SiO_2 (or equivalent oxide) thickness with device scaling (technology generation). Actual or expected year of implementation of each technology generation is indicated [adapted from ITRS (Ref. 16)].

from hundreds of nanometers (nm) 40 years ago to less than 2 nm today, to maintain the high drive current and gate capacitance required of scaled MOSFETs. Further, as can be seen in Fig. 3, SiO_2 thickness continues to shrink. Many ultrasmall transistors have been reported, with SiO_2 layers as thin as 0.8 nm.[9–15] The International Technology Roadmap for Semiconductors,[16] excerpted in Table II, shows that SiO_2 gate dielectrics of 1 nm or less will be required within 10 years. [It will become obvious while reading this article that SiO_2 layers thinner than ~1.2 nm may not have the insulating properties required of a gate dielectric. Therefore alternate gate dielectric materials, having "equivalent oxide thickness" less than 1.2 nm (for example), may be used. Equivalent oxide thickness, $t_{ox}(\text{eq})$, is the thickness of the SiO_2 layer ($\kappa=3.9$) having the same capacitance as a given thickness of an alternate dielectric layer, t_{diel} ($\kappa=\kappa_{\text{diel}}$). Equivalent oxide thickness is given by the relationship: $t_{ox}(\text{eq})=t_{\text{diel}}(3.9/\kappa_{\text{diel}})$.] At these thicknesses, the Si/SiO_2 interface becomes a more critical, as well as limiting, part of the gate dielectric. A 1 nm SiO_2 layer is mostly interface, with little if any bulk character. It contains about five layers of Si atoms, at least two of which reside at the interface.[17] Given its prominence, much of this article will focus on the physical and electrical properties of the Si/SiO_2 interface.

Due to its commercial relevance, the Si/SiO_2 system has received an enormous amount of scientific attention. It is daunting to count the number of scientific papers: using an INSPEC Database we found 36 708 references (since 1969) devoted to this system. [We intersected the set "silicon" with the set "(SiO or SiO_2 or SiO_x)" and then subtracted the set "quartz."] Only 2% of these references are cited in this article. Several excellent books[18–23] and review papers on dielectric selection,[24] atomic scale interactions between Si and O,[25–27] oxidation of Si,[28–30] SiO_2 structure,[31] interface structure and defects,[32–34] reliability,[35] metrology,[36] Si–O–N,[2,37,38] and general growth, structure and properties[39,40] have been published. However, some basic scientific issues at the forefront of the field remain unresolved. Among these issues are an understanding of the exact diffusion mechanisms and incorporation reactions of oxidizing and nitriding species in SiO_2, an atomistic understanding of the initial stages of oxidation, the role of postoxidation processing on physical and electrical properties, the bonding structure at and near the Si/SiO_2 interface, the relationship between local bonding/chemistry and electrical defects, and the failure mechanisms in ultrathin dielectrics. All of these topics will be addressed in this article.

It is amusing and instructive to learn that not only is SiO_2 enabling to microelectronics, but also to some forms of life itself. Many forms of animal and plant life have cell membranes and exoskeletons composed of pure, crystalline (opaline) SiO_2.[41] This should not be too surprising, since Si and O are the two most abundant elements in the earth's crust. In particular, one celled animals called diatoms fashion their cell membrane via self-assembly (molecule by molecule), from SiO_2 dissolved in H_2O, at ambient temperature.[42] They exist in thousands of symmetric morphologies. Figure 4 is a scanning electron microscopy image of the SiO_2 exoskeleton of a diatom, on which one can ob-

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

TABLE II. MOSFET technology timetable, adapted from the International Technology Roadmap for Semiconductors (ITRS) (Ref. 16).

First year of production	1999	2001	2002	2005	2008	2011	2014
DRAM generation	1G	1G	4G	16G	64G	256G	1T
Minimum feature size, nm	180	160	130	100	70	50	35
Equivalent oxide thickness, nm	1.9–2.5	1.5–1.9	1.5–1.9	1.0–1.5	0.8–1.2	0.6–0.8	0.5–0.6

serve SiO_2 features as small as 100 nm. It is humbling to discover that diatoms evolved with such ''scaled dimensions'' 400 million years ago, and suggests that in the future, SiO_2, as well as other electronic materials structures, might be self-assembled by biomimetic processes. In fact, such structures have already been achieved.[43,44]

B. Fundamental limits of SiO_2: Is the end in sight?

The use of ultrathin SiO_2 gate dielectrics gives rise to a number of problems, including high gate leakage current, reduced drive current, reliability degradation, B penetration, and the need to grow ultrathin and uniform SiO_2 layers. We may ask when any of these effects will fundamentally limit the usefulness of SiO_2 as a gate dielectric.[45]

Due to the large band gap of SiO_2, ~9 eV, and the low density of traps and defects in the bulk of the material, the carrier current passing through the dielectric layer is normally very low. For ultrathin films this is no longer the case. When the physical thickness between the gate electrode and doped Si substrate becomes thinner than ~3 nm, direct tunneling through the dielectric barrier dominates leakage current.[11,40,46–48] According to fundamental quantum-mechanical laws, the tunneling current increases exponentially with decreasing oxide thickness. Gate leakage currents measured on 35 nm transistors fabricated using advanced wafer preparation, cleaning, and oxidation procedures[14] are shown in Fig. 5. The leakage current is seen to increase by one order of magnitude for each 0.2 nm thickness decrease.

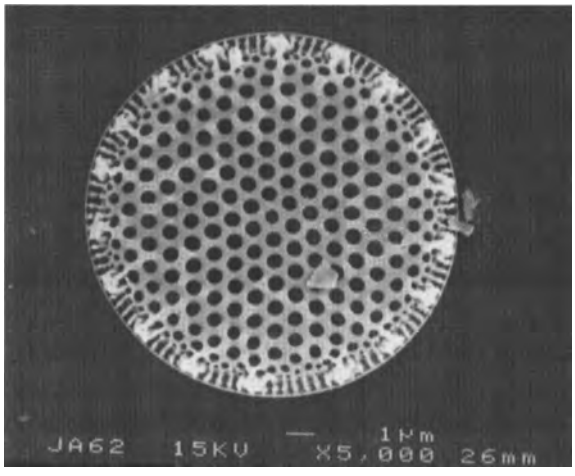


FIG. 4. Scanning electron microscope image of a diatom exoskeleton, composed of opaline SiO_2 (courtesy of J. Aizenberg, Bell Laboratories/Lucent Technologies).

Assuming a maximum allowable gate current density of 1 A/cm^2 for desktop computer applications, and 10^{-3} A/cm^2 for portable applications, minimum acceptable SiO_2 thicknesses (physical) would be approximately 1.3 and 1.9 nm, respectively.

Recent electron energy loss spectroscopy (EELS) experiments on ultrathin Si/SiO_2 interfaces, in a scanning transmission electron microscope (STEM), support these findings.[17] Oxygen profiles across the interface were obtained and are shown in Fig. 6 for SiO_2 films 1.0 and 1.8 nm thick. The profiles consist of bulk-like regions and interfacial regions, and the interfacial regions are thought to be due to interfacial states. Based on this analysis, it has been calculated that the minimum oxide thickness, before leakage current becomes overwhelming, is 1.2 nm. This comes from the fact that a satisfactory SiO_2 tunnel barrier is formed when it is equal in thickness to six times the decay length of the interfacial states, about 6×0.12 nm$\cong$0.7 nm, plus a 0.5 nm contribution from interfacial roughness.

Reduced drive (drain) current has been reported in small transistors with ultrathin gate dielectrics.[10] Figure 7 shows that drain current increases with decreasing SiO_2 thickness, but then falls off; gate leakage current continuously increases, as expected, with decreasing SiO_2 thickness. Thus for SiO_2 layers thinner than about 1.3 nm there is no advan-

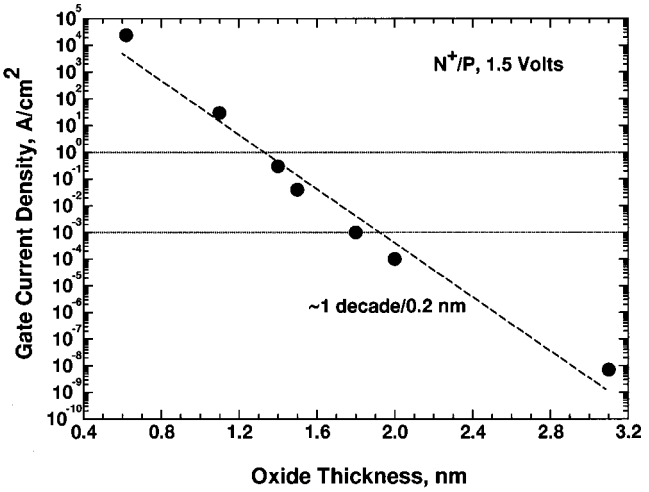


FIG. 5. Gate leakage current measured at 1.5 V as a function of oxide thickness (measured by TEM) for 35 nm NMOSFETs. Leakage current increases one order of magnitude for every 0.2 nm decrease in SiO_2 thickness. Horizontal lines indicate 1 A/cm^2 acceptable leakage current for desktop applications, and 1 mA/cm^2 acceptable leakage for portable applications [data of G. Timp, from Green *et al.* (Ref. 45)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

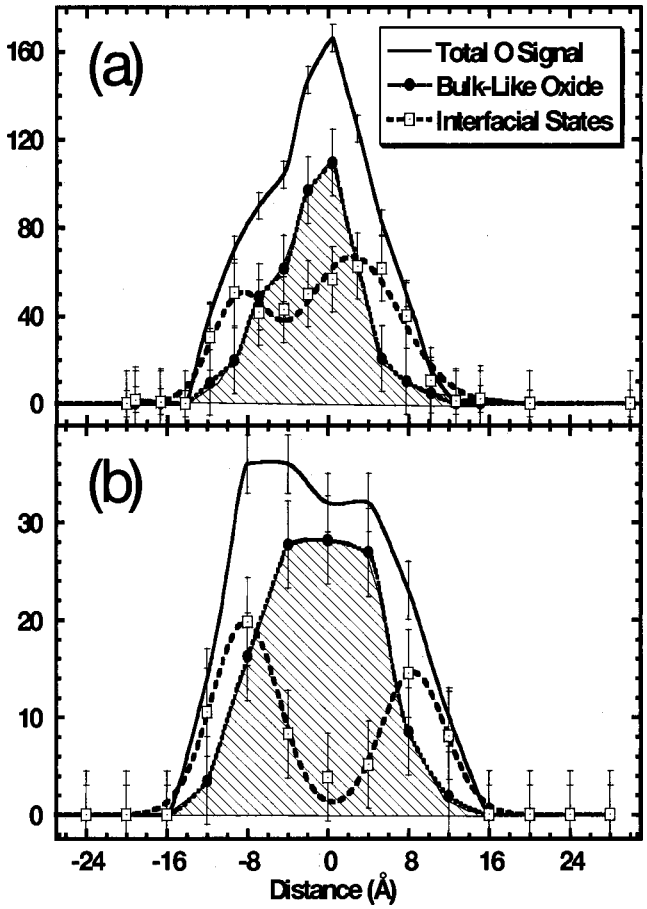


FIG. 6. Oxygen bonding profiles measured by STEM-EELS. The Si substrate is on the left and the gate polycrystalline Si is on the right. (a) 1.0 nm (ellipsometric) oxide, annealed at 1050 °C/10 s. The bulk-like O signal (*y* axis, arbitrary scale) yields a FWHM of 0.85 nm, whereas the total O signal yields a FWHM of 1.3 nm. The overlap of the two interfacial regions has been correlated with the observation of a very high gate leakage current, 10^2 A/cm^2. (b) a thicker (1.8 nm ellipsometric) oxide, also annealed. The interfacial regions no longer overlap and the gate leakage current is 10^{-5} A/cm^2 [from Muller *et al.* (Ref. 17)].

tage in performance (drive current) for incurring the burden of an ever-increasing gate leakage current. This would suggest that SiO_2 layers thinner than 1.3 nm no longer deliver any performance advantage. The cause of the decreased

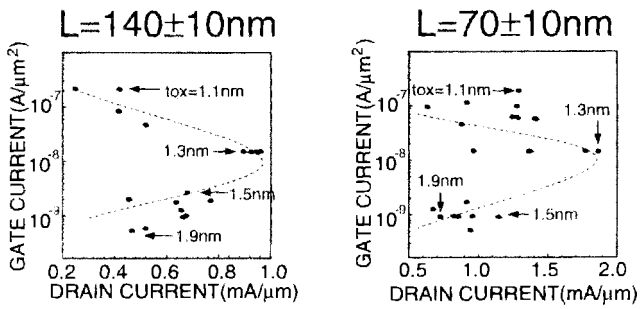


FIG. 7. Drive current vs leakage current for two ultrasmall (gate lengths of 70 and 140 nm) NMOSFETs. In both cases it can be seen that gate current increases, as is expected, with decreasing SiO_2 thickness. However, drain current first increases and then falls off with decreasing oxide thickness. Decreasing the oxide thickness past the fall-off thickness confers no further advantage on the device [from Timp *et al.* (Ref. 10)].

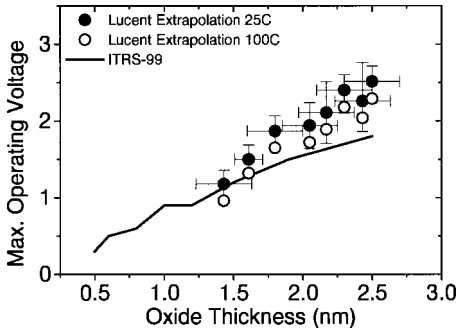


FIG. 8. Predicted maximum allowable operating voltage as a function of oxide thickness (Ref. 16) (solid line), modeled so that requirements of power dissipation and circuit speed for successive technology generations are met. The Lucent data, at either 25 or 100 °C, estimates the safe operating voltages (for 10 year lifetime reliability) for sub-2.5 nm oxides, based on measured results and extrapolation principles (Ref. 62). The Lucent data clearly show that the 10 year reliability of sub-2.5 nm oxides meets the ITRS specifications for SiO_2 layers as thin as 1.4 nm.

drive current is not fully understood. One possibility is an additional scattering component from the upper (SiO_2/polycrystalline Si gate) interface. Some experimental evidence exists for this case[49] but the observed effect is not enough to explain the data in Fig. 7. Another cause could be a universal mobility curve effect, i.e., lowered mobility due to enhanced scattering because of extreme carrier confinement in the inversion layer of the ultrathin oxide. The issue of long-range electrostatic interactions between charges in very heavily doped gate, source, and drain regions, and electrons traveling in the channel, was recently theoretically studied[50] using both semiclassical two-dimensional self-consistent Monte Carlo–Poisson simulations and a quantum mechanical model based on electron scattering from gate–oxide interface phonons. It was shown that excitation and absorption of plasma modes in the gate region may result in a net momentum loss of carriers in the channel, thus decreasing their velocity, and leading to reduced drain current.

Reliability (lifetime to breakdown) of ultrathin SiO_2 is a major concern for oxide scaling into the sub-2 nm range and currently a contentious issue.[35,40,51–62] Electrons traveling through the SiO_2 layer may create defects such as electron traps and interface states[63–65] that in turn, upon accumulation to some critical density, degrade the insulating properties of the oxide. The accumulated charge the film can withstand before its breakdown (Q_{bd}) decreases with oxide thickness.[54] Recently, it was predicted that oxide films thinner than about 2.2 nm would not have the reliability required by the industry roadmap.[54] Data from another research group,[62] shown in Fig. 8, indicates that acceptable reliability will be achievable for SiO_2 thicknesses as low as 1.4 nm. At about 1.0 nm thickness, the statistical probability of a percolation path may reduce reliability to an unacceptable level.[66] One should mention that all reliability data is model dependent. Unlike directly measured parameters such as the gate leakage and drive currents, reliability studies always involve extrapolations from relatively high (~2.5–4 V) stress voltages to real device operating voltages (~1.0–1.2 V). The extrapolations are based on different, although most often percolation type, models with several parameters extracted from the high

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

stress voltage experiments. Finally, the real impact of oxide breakdown on circuit performance, which ultimately is the critical issue, has yet to be understood.

Thus the fundamental limits imposed on SiO_2 are excessively high gate leakage current, reduced drive current, and reliability. The first two of these properties impose a limit of ~1.3 to 1.4 nm as the thinnest SiO_2 acceptable. Although potential improvements in interfacial roughness may push the leakage limit to ~1.0 nm, reliability may then be the limiting factor. Complementary metal–oxide–semiconductor (CMOS) applications of SiO_2 or Si–O–N gate dielectrics are limited neither by the ability to grow the ultrathin films in a manufacturing environment (see Sec. IV), nor to suppress the diffusion of B through them (see Sec. VI). Therefore, according to Table II, SiO_2 will have to be replaced in as little as 5 years if gate capacitance is to increase according to projected scaling. Technology generations that require <1.0 nm equivalent SiO_2 thickness will have to rely on alternate, high-κ gate dielectrics (see Sec. VII). This transition will not be simple to implement, as SiO_2 is the major reason that silicon technology has been so successfully integrated thus far. One can say that SiO_2 has only one disadvantage, low κ, and most alternate gate dielectrics currently have only one advantage, high κ.

In this introductory section we have systematically examined the repercussions of decreasing SiO_2 gate dielectric thickness on several physical and electrical parameters. Although the end of SiO_2 scaling may be in sight, it will be manufactured in integrated circuits for at least the next decade. This article is not intended to be an obituary for SiO_2, however, since its useful life will undoubtedly be extended by innovations in device design, e.g., dual gate dielectric thickness devices[67,68] or vertical MOSFETs.[69]

II. PHYSICAL CHARACTERIZATION METHODS FOR ULTRATHIN DIELECTRICS

In this section we will briefly introduce the various analytical techniques useful for studying the physical properties, such as thickness, composition, density, crystallinity, bonding, and surface and interface morphology, of ultrathin gate dielectrics. We will overview only the basic principles of the techniques, the information they yield, and their strengths and limitations. The techniques are grouped into the following categories: optical, x-ray, ion beam, electron beam, and scanning probe microscopy. Each technique will be represented by important dielectric results. Our choice of techniques is not exhaustive, but primarily reflects our perception of the impact of the various techniques on the understanding of the field.

A. Optical methods

The most commonly used optical techniques are single wavelength and spectroscopic ellipsometry,[29,70–85] reflectance difference spectroscopy (RDS),[86–88] second harmonic generation (SHG),[89–97] and Fourier transform infrared spectroscopy (FTIR).[82,98–107]

Ellipsometry is based on the measurement and subsequent modeling of changes in the polarization state of a light beam reflected from a sample surface, as is illustrated in Fig. 9. The measured parameters are the ellipsometric angles Ψ and Δ, defined from the ratio

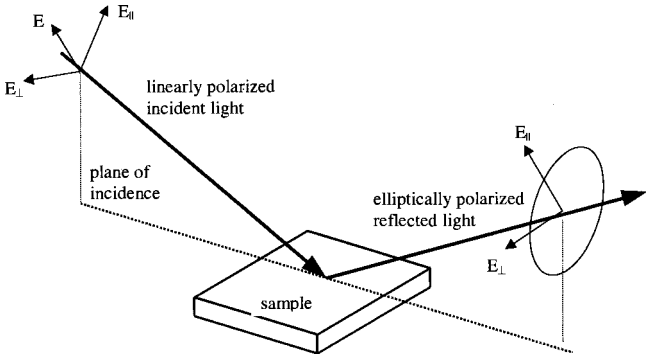


FIG. 9. Principles of an ellipsometric measurement.

$$R_{\parallel}/R_{\perp} = \tan(\Psi)\exp(i\Delta) \tag{1}$$

of the Fresnel reflection coefficients $R_{\parallel}$ and $R_{\perp}$ for the light polarized parallel and perpendicular to the plane of incidence. The reflection coefficients are determined by the optical properties and composition of the substrate and overlayers, their thicknesses, and morphology. The parameters Ψ and Δ can be measured either at a given wavelength of light, i.e., single wavelength ellipsometry (most often 633 nm), or as a function of photon energy, i.e., spectroscopic ellipsometry. The single wavelength configuration is often used for fast, nondestructive, on-line monitoring of film thickness, provided that the refractive index of the film is known. The spectroscopic mode allows determination of the refractive index (η) as well as the thickness. For SiO_2 films on Si, good agreement has been demonstrated, Fig. 10, between the ellipsometric oxide thickness and thickness values determined by transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS), for films as thin as ~2 nm.[108] Since the very first publications on Si oxidation, ellipsometry

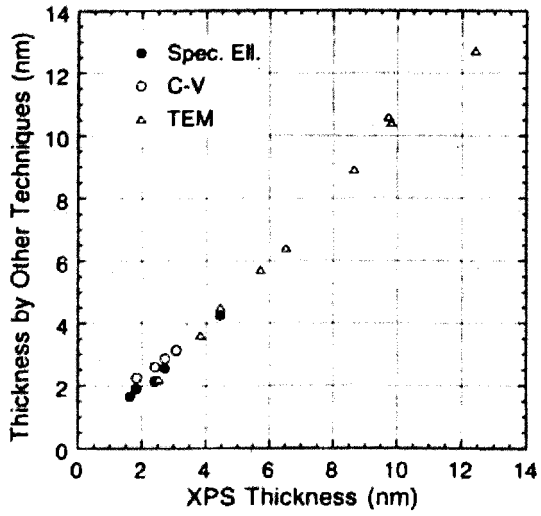


FIG. 10. Oxide thickness measured by x-ray photoemission spectroscopy, compared to measurements on the same films by ellipsometry, transmission electron microscopy, and capacitance–voltage techniques [from Lu *et al.* (Ref. 108)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

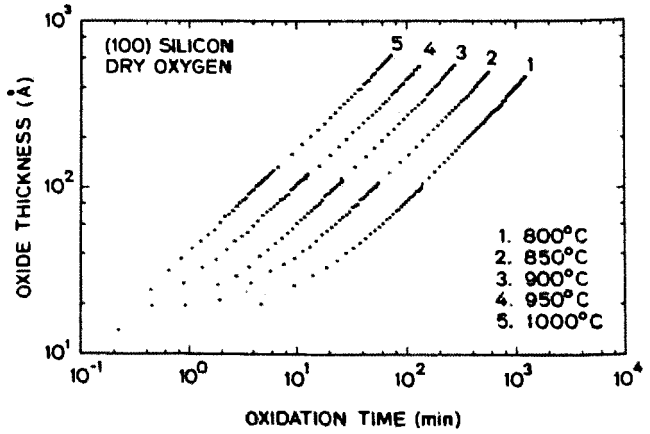


FIG. 11. Si(100) oxidation kinetics at different temperatures, as measured by high temperature ellipsometry [from Massoud *et al.* (Ref. 73)].

has been the tool of choice to measure film thickness. Knowledge of the thickness is critical in modeling oxidation kinetics and determining growth mechanisms.[29] An example of its application is shown in Fig. 11.

The ellipsometric parameters, Ψ and Δ, can be detected with very high accuracy, making ellipsometry one of the most sensitive thickness measurement techniques. However, the interpretation of the measurements is very model dependent, especially in the ultrathin regime where η may become, as is the case for SiO_2, a function of thickness.[78,109,110] For more complex gate dielectrics such as Si–O–N or SiO_2/Si_3N_4 multilayer stacks, the analysis is further complicated by the fact that η changes with the composition of the film.[111,112] For example, at a wavelength of 630 nm, η varies linearly with the amount of N in the film, Fig. 12, from a value of 1.46 for SiO_2 to a value of approximately 2.0 for stoichiometric Si_3N_4.[111]

Sensitivity to the Si/SiO_2 interface of ultrathin films is relatively low using conventional ellipsometric configurations. Interfacial sensitivity can be enhanced via an immersion ellipsometry technique, in which the Si/SiO_2 sample is placed in a liquid having an η close to that of SiO_2, thereby

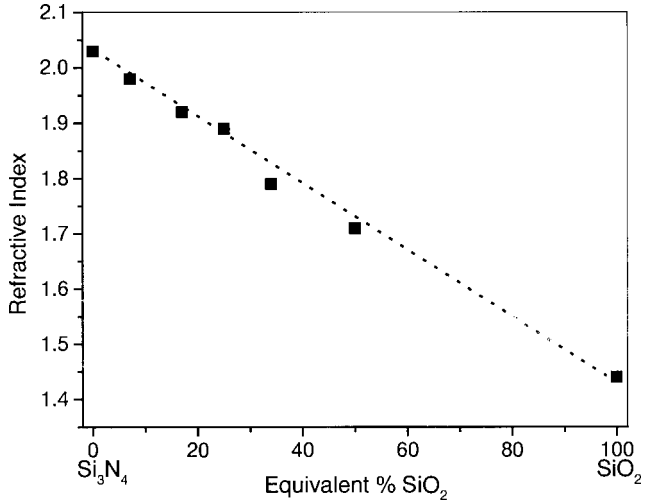


FIG. 12. Refractive index of Si–O–N layers as a function of composition [adapted from data in Brown *et al.* (Ref. 111)].

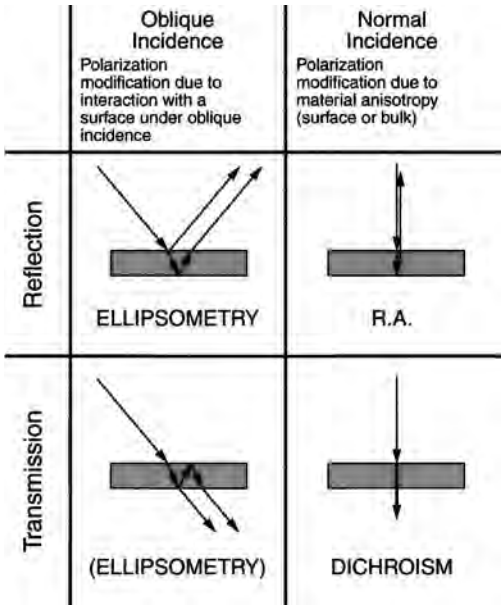


FIG. 13. Schematic illustrations of various polarized light methods for thin film characterization [adapted from Drevillon *et al.* (Ref. 88)].

effectively increasing the optical thickness of the oxide overlayer.[75,113] Sensitivity to surfaces and interfaces may also be significantly enhanced using RDS. While in conventional ellipsometry the measurements are performed under oblique incidence, in RDS the primary photon beam is normal to the surface, as is illustrated in Fig. 13. The analysis is based on the determination of the reflectance differences of the light polarized along principle axes of the crystal surface. The anisotropic properties of surfaces and interfaces can therefore be determined. RDS has been applied to the study of Si oxidation as well as the wet cleaning of Si.[86,87] Details of the RDS technique and its application to semiconductor surfaces and interfaces have recently been reviewed.[88]

Another important method for the selective optical probing of surfaces and interfaces is SHG.[89–97] In general, the polarization amplitude, P, of a photon beam of optical frequency ω, interacting with a solid sample, can be expressed in terms of an expansion over the amplitude of the electromagnetic field (E), as

$$P \sim \alpha(\omega)E(\omega) + \beta(\omega,2\omega)E^2(\omega) + \cdots . \tag{2}$$

The first term of the polynomial expansion represents the linear optical response, which is the basis of the ellipsometric and RDS techniques described above. In centrosymmetric solids such as Si, the second, nonlinear coefficient β is nonzero only at interfaces, where crystal symmetry is broken. The electrical dipoles present at such interfaces give rise to the surface/interface selectivity of SHG. Recently, SHG generation methods have been used to investigate the structure of Si/SiO_2 and Si/Si_3N_4 interfaces, Fig. 14, as well as the initial stages of Si oxidation in N_2O and O_2.[89–92,95,96]

FTIR is a powerful method to examine chemical (stoichiometry, bonding and impurities), and structural (stress, transitional layer) aspects of ultrathin dielectric films.[82,98–106,114,115] The technique, based on the absorption of light in the infrared region of the spectrum, is sensitive to

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

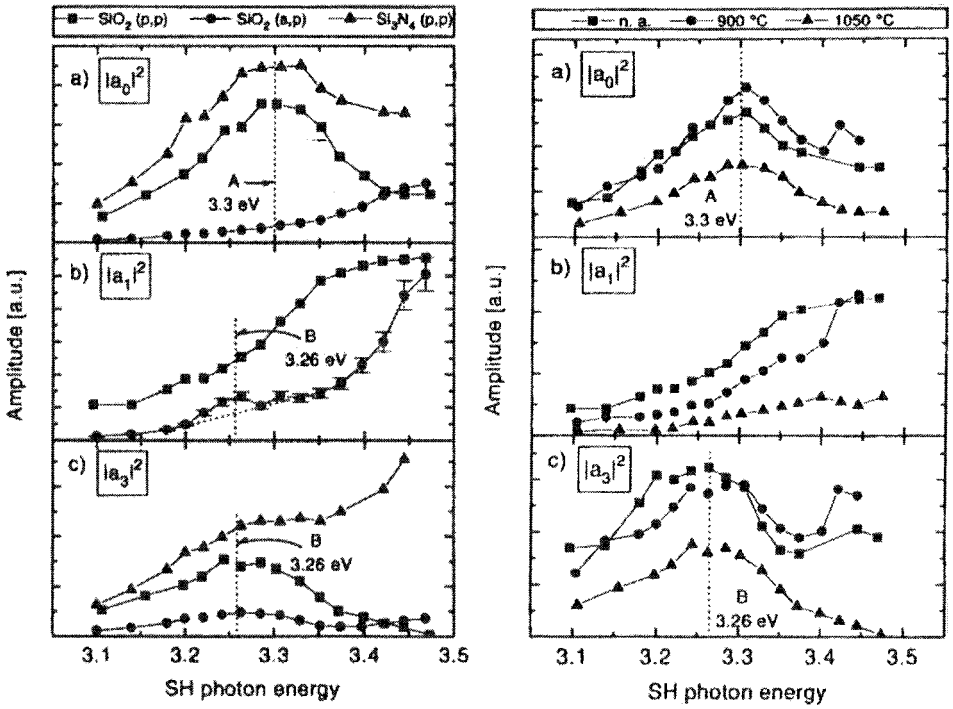


FIG. 14. Second haromonic generation measurements (*y* axis, arbitrary units), as a function of photon energy, for $Si(111)/Si_3N_4$ and $Si(111)/SiO_2$ interfaces (left panel), and the effect of annealing on the $Si(111)/SiO_2$ interface (right panel) [from Meyer *et al.* (Ref. 94)].

rotational, bending, and stretching vibrational modes, and therefore can probe local atomic configurations and compositions. It is one of a few techniques that can be used to study the behavior of H on Si surfaces and interfaces,[116–118] as is illustrated, for example, in Fig. 15. The spectrum of Si–O stretching vibrations in an amorphous SiO_2 oxide film is characterized by two bands, designated transverse optical (TO) and longitudinal optical (LO), polarized parallel and perpendicular to the plane of the film, respectively;[115,119] this is exemplified in Fig. 16. Unfortunately, the bands may be broad, which complicates their interpretation. Detailed analysis of the relative intensities and TO/LO peak positions (1065/1252 cm^{-1}, respectively, for Si–O), based on recent theoretical and experimental findings is given in a recent review.[36] It has also been shown that both TO and LO bands show a shift to lower wave numbers with decreasing oxide thickness, usually attributed to the presence of Si suboxides near the Si/SiO_2 interface.[36] In the case of NO and N_2O grown Si–O–N films, in addition to the above TO and LO bands of the oxide, a peak at 960 cm^{-1} has been observed, distinct from the vibrational frequency at 840 cm^{-1} characteristic of Si_3N_4.[120] This peak has been attributed to the asymmetric stretching vibration of double-bonded N atoms in the Si–N–Si structure. In Fig. 17 it is shown that IR methods have also been used to study composition and thickness of SiO_x films at the interface of Ta_2O_5 and other oxide films deposited on Si, and the evolution of such layers upon thermal treatment.[103,107]

B. X-ray based methods

Higher energy photon-based methods (x-ray analyses) are widely used to determine chemical and structural properties of ultrathin dielectrics and their interfaces. X-ray photoemission spectroscopy (XPS) is a common technique used to determine local chemical environment.[121–126] XPS analy-

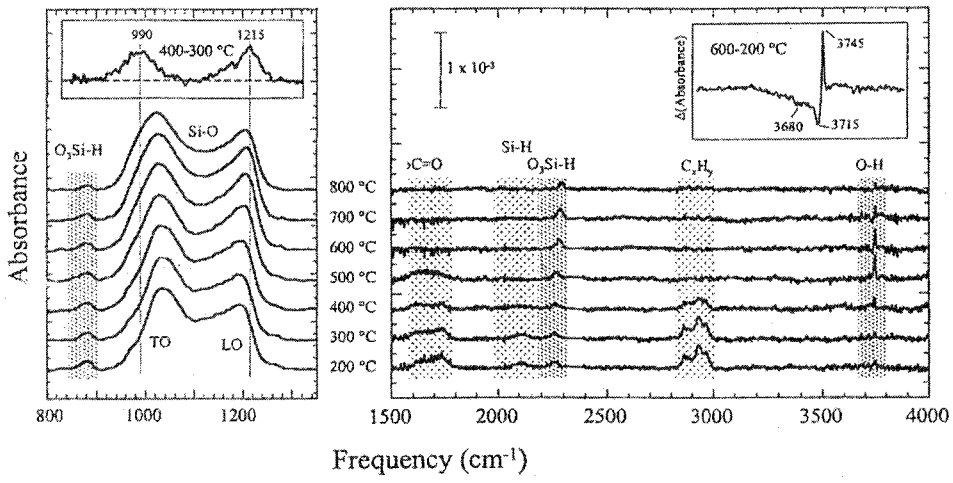


FIG. 15. Example of the use of Fourier transform infrared spectroscopy (absorbance as a function of frequency) to study H binding on a partially oxidized Si surface [from Gurevich *et al.* (Ref. 747)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

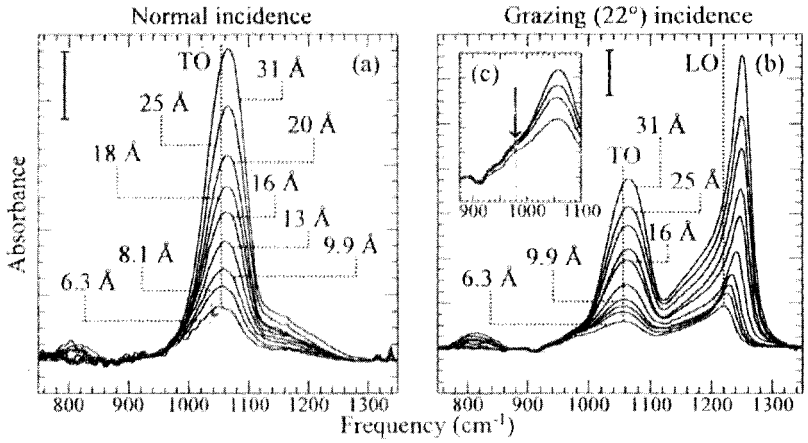


FIG. 16. Thickness dependence of the transverse optical and longitudinal optical modes of SiO_2 (on Si), as measured by Fourier transform infrared spectroscopy [from Queeney *et al.* (Ref. 119)].

sis is based on the fact that core electron energies are characteristic of the emitting atom. For any given atom, exact core level positions, the so-called chemical shifts, change with local chemical environment. The analysis of photoemission from the Si $2p$ core level has been used to investigate the structure of the Si/SiO_2, Si/Si_3N_4, and Si/SiO_xN_y interfaces,[27,121,122,124,127–140] defect states in dielectric films,[141,142] valence band alignment,[143–145] and the initial stages of oxidation.[27,146–162] The Si $2p$ level for Si atoms in stoichiometric SiO_2, with all Si atoms in an $Si(-O)_4$ tetrahedral configuration, is shifted to ~4 eV deeper binding energy with respect to the position of the level in elemental Si. Photoemission yields of much lower intensity, at energies between the SiO_2 line and substrate Si, Fig. 18, have also been observed. These are usually interpreted in terms of suboxide (Si^{+1}, Si^{+2}, and Si^{+3}) states at the interface or in the film,[122,124,129,130,163–165] as can be seen in the compilation in Table III. More recently this traditional interpretation has been questioned.[133,136,139,166,167] It has been argued that second nearest neighbor effects can lead to additional shifts of Si $2p$ levels, making quantitative analysis of suboxide states even more complicated. In either case, current estimates of the total concentration of Si in the suboxide states are between one and two monolayers, whereas an atomically abrupt interface would result in one monolayer of suboxide. [A monolayer of a species on Si(100) represents a concentration of $6.8\times10^{14}\,cm^{-2}$, assuming no steric hindrance.] An example of a new approach to analysis of the Si/SiO_2 interface is depicted in Fig. 19. XPS is also useful in obtaining film thickness, determined by the Si($2p$) mean free path and the ratio of Si $2p$ peaks corresponding to SiO_2 in the film and Si in the substrate.[121]

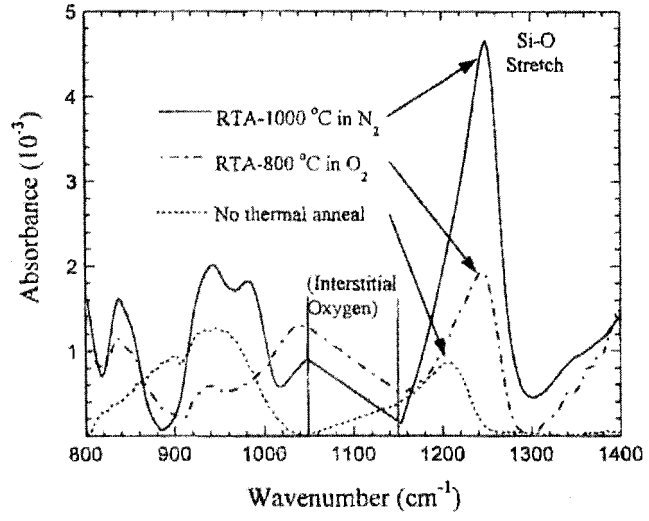


FIG. 17. Fourier transform infrared spectra of the Ta_2O_5/Si system showing the progression of absorbance features in the Si–O stretch region, following various anneals [from Alers *et al.* (Ref. 103)].

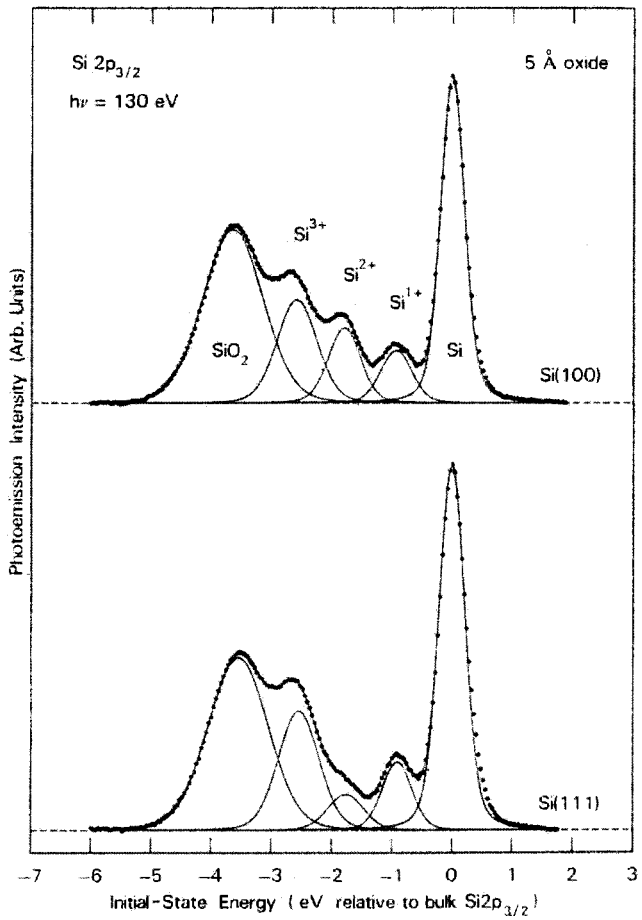


FIG. 18. Synchrotron-based Si $2p$ x-ray photoemission spectra for $Si(100)/SiO_2$ and $Si(111)/SiO_2$ interfaces [from Himpsel *et al.* (Ref. 130)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

TABLE III. Summary of XPS Si $2p$ analyses for the Si/SiO_2 system.

(1) Chemical shifts with respect to the Si substrate (Si^0) peak, in eV, assuming five (Si^0,Si^{1+},Si^{2+},Si^{3+},Si^{4+}) components of the Si $2p$ spectra. Second nearest neighbor effects [Banaszak-Holl *et al.* (Ref. 136] are not considered.

Reference	Si^{1+}	Si^{2+}	Si^{3+}	Si^{4+}
130	0.95	1.75	2.48	3.90
132	1.00	1.65	2.50	4.00
743	0.95–1.00	1.72	2.50	3.60
134	0.98	1.82	2.65	3.84
138	0.97	1.73	2.58	3.57
744	0.94–0.95	1.78–1.80	2.50–2.56	4.00–4.04

(2) Intensities of different oxidation states: $I(Si^0)+I(Si^{1+})+I(Si^{2+})+I(Si^{3+})+I(Si^{4+})=100\%$ at a photon energy of 200 eV, for different oxide film thicknesses, from Tao *et al.* (Ref. 744). [Note: $I(SiO_x)$=total XPS intensity from Si^{1+}, Si^{2+}, and Si^{3+} suboxide states.]

Film (nm)	$I(Si^0)$	$I(Si^{1+})$	$I(Si^{2+})$	$I(Si^{3+})$	$I(Si^{4+})$	$I(SiO_x)/I(Si^0)$
0.9	11.53	1.91	1.46	2.82	82.29	0.54
1.5	5.99	1.06	0.96	1.67	90.32	0.61
1.8	3.64	0.31	0.76	0.75	94.04	0.50

Also, Tao *et al.* (Ref. 744), for a 0.9 nm film at different photon energies.

Energy (eV)	$I(Si^0)$	$I(Si^{1+})$	$I(Si^{2+})$	$I(Si^{3+})$	$I(Si^{4+})$	$I(SiO_x)/I(Si^0)$
130	3.95	0.79	0.89	2.01	92.36	0.93
150	7.29	1.35	1.28	2.70	87.38	0.76
200	11.53	1.91	1.46	2.82	82.29	0.54

Early XPS studies of Si–O–N films were limited to the detection of N at the interface of samples annealed in N.[168] More recent high resolution photoemission studies of N(N $1s$) core levels were useful in understanding N bonding and depth distribution, using either HF etch back or variable photoelectron takeoff angle methods.[2,126,135,137,157,162,169–172] Assignments of N $1s$ peaks are indicated in Table IV, based on theoretical Si–N and Si–O–N bonding configurations depicted in Fig. 20. Depth analysis via XPS requires knowledge of the escape depths of the N $1s$ or Si $2p$ photoelectrons, which are on the order of 2.0–3.5 nm for conventional Al $K\alpha$ or Mg $K\alpha$ x-ray sources. A detailed analysis of the N $1s$ peak shape shows that the peak is asymmetric and consists of several components. Evidence for this can be found in Figs. 21 and 22.

TABLE IV. Summary of N $1s$ XPS analysis. Multiple (at least two) local electronic configurations of N atoms are observed in the films.

N $1s$ peak at ~397.6 eV
located closer to the interface (Ref. 2) N triple bonded to Si, i.e., as in Si_3N_4 (Ref. 137)
N $1s$ peak(s) at ~398.3–399 eV
located further into the film (Ref. 158) less straightforward interpretation (N double bonded to Si, N–O bonds, strained bonds, second neighbor effects) (Ref. 745) shifts with film thickness (Ref. 746)
N $1s$ peak(s) at >400 eV
due to metastable bonding configurations of N (Ref. 172)

X-ray scattering techniques have also been successfully used to study various structural aspects of ultrathin oxide films on Si, including interface roughness,[173–183] variations in oxide density in the ''bulk'' of the film and near the interface,[184] and ordered structures near the interface.[185–189] The state of order at the interface is still a matter of debate and will be discussed in more detail in Sec. V.

X-ray diffraction crystal-truncation (CTR) profiling has been developed to measure roughness at buried interfaces, so that the SiO_2 layer need not be etched off.[173–175] In the case of an amorphous overlayer, the variation of x-ray diffracted intensity along the truncated rod provides information about the root mean square value of roughness at the interface. Since the diffraction from the interface is rather weak, the

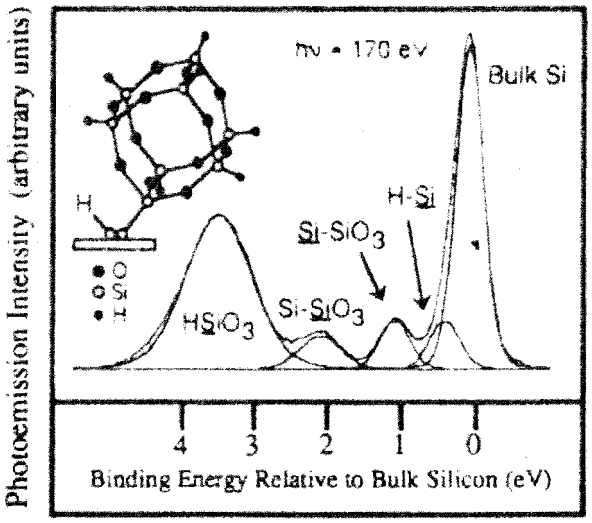


FIG. 19. Si $2p$ core level x-ray photoemission spectrum of the model interface derived from $H_8Si_8O_{12}$ clusters on Si, showing peak assignments [from Banaszak-Holl *et al.* (Ref. 136)].

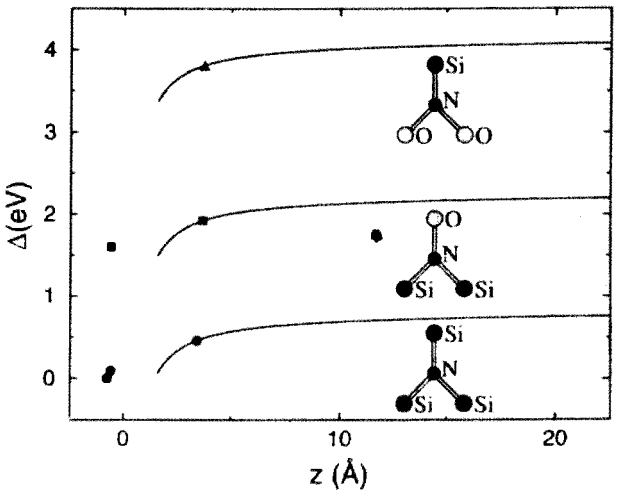


FIG. 20. N $1s$ core level x-ray photoemission spectrum shifts at $Si(100)/SiO_2$ interfaces, calculated for $N–Si_3$ (circle), $N–Si_2O$ (square), and $N–SiO_2$ (triangle) configurations, as a function of distance, z, from the interface [from Rignanese *et al.* (Ref. 748)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

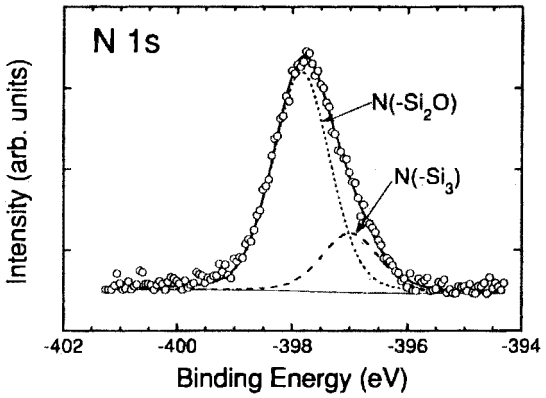


FIG. 21. N 1*s* core level x-ray photoemission spectrum for a Si–O–N film thermally grown in N_2O, showing contributions from N–Si_3 and N–Si_2O bonds [from Lu *et al.* (Ref. 137)].

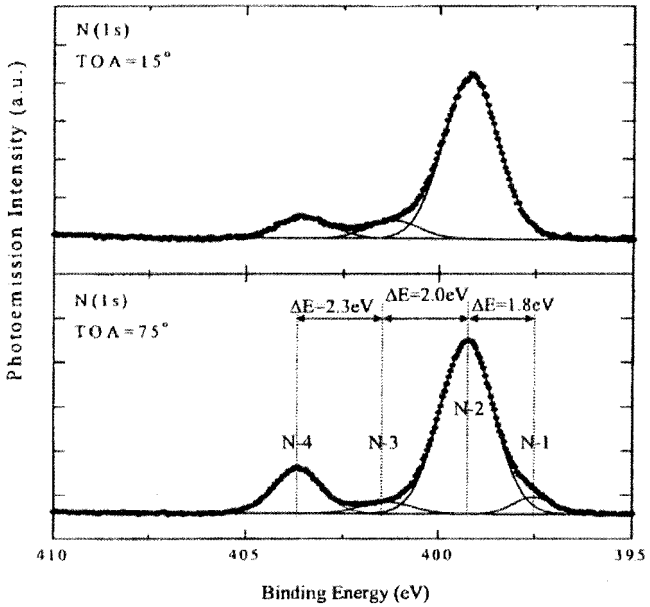


FIG. 22. N 1*s* core level x-ray photoemission spectra of an unannealed, plasma-deposited 4 nm Si–O–N film, at 15° and 75° takeoff angles. Four distinct chemical bond states for nitrogen are observed [from Chang *et al.* (Ref. 172)].

experiment is best performed with a synchrotron radiation source. X-ray diffraction measures the Fourier transform of the electron density. By measuring and modeling intensity profiles, one can obtain statistical information about the smoothness of the interface. The technique has been used to explore the quality of the interface as a function of processing parameters such as growth temperature, Fig. 23, and interface nitridation.[173–175,190] It has also been demonstrated that CTR results correlate well with roughness measurements deduced from the SHG technique.[191]

X-ray reflectivity is another method for studying the interface, since the reflectivity represents the Fourier transform of the spatial derivative of the sample density in the perpendicular direction. Modeling x-ray reflectivity spectra with film thickness and density as fitting parameters yields information about structural properties of oxide films. In a recent study of thin rapid thermal oxides (RTO), Fig. 24, the best fit to the data was found using a two layer model, the thin (~1.5 nm) interfacial oxide layer being slightly denser than the overlying ''bulk'' oxide layer.[184]

C. Ion beam analysis

The family of ion beam based techniques includes Rutherford backscattering spectroscopy (RBS),[192–195] medium energy ion scattering spectroscopy (MEIS),[2,103,196–209] nuclear reaction analysis (NRA),[25,37,210–226] and secondary ion mass spectroscopy (SIMS).[227–233] These techniques provide very accurate determinations of composition and distribution of Si, O, N, and other elements in dielectrics.

In RBS, a high energy ion beam (typically H^+ or He^+, with greater than MeV energy), scatters off the target. The scattering event is described by a Coulomb interaction, the cross-section of which is well known. The energy of the backscattered ions is determined by the energy of the incident particles, the masses of the primary ions and the target atoms, and the scattering geometry, all based on a binary collision model. Typical backscattering data is illustrated in Fig. 25. The integrated area of a backscattered peak can be easily converted into a concentration of a particular element in the target, as is done for the case of SiO_2 films in Fig. 26. Experiments can be performed in either random or channeling scattering geometries. In the channeling geometry, the ion beam is aligned along a crystallographic direction of the target substrate. This significantly reduces the background scattering from the substrate and increases sensitivity to the overlayer. Since impinging particles in the MeV energy range lose relatively little energy upon scattering, energy shifts of the backscattered peaks will be small compared to the energy resolution of the solid state detectors used in RBS experiments. The result is that RBS has relatively poor depth resolution, i.e., 10 nm or greater, and is therefore not useful in the ultrathin dielectrics regime, although depth resolution

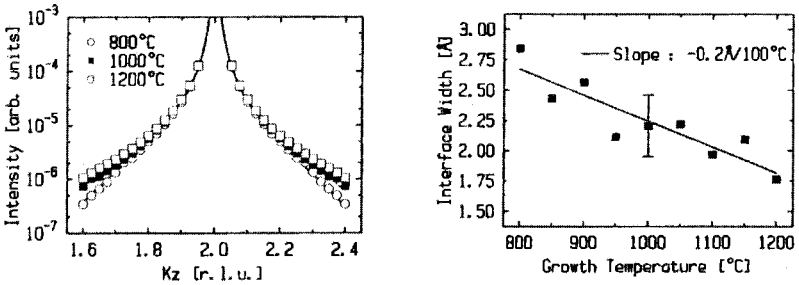


FIG. 23. Synchrotron x-ray diffraction studies of the Si/SiO_2 interfaces of ~10 nm SiO_2 gate oxides grown at different temperatures. The left panel shows the intensity for the $(20\,K_z)$ diffraction rod. The right panel demonstrates how the interface width (deduced from the fit of the experimental results shown on the left) changes as a function of growth temperature [from Tang *et al.* (Ref. 175)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

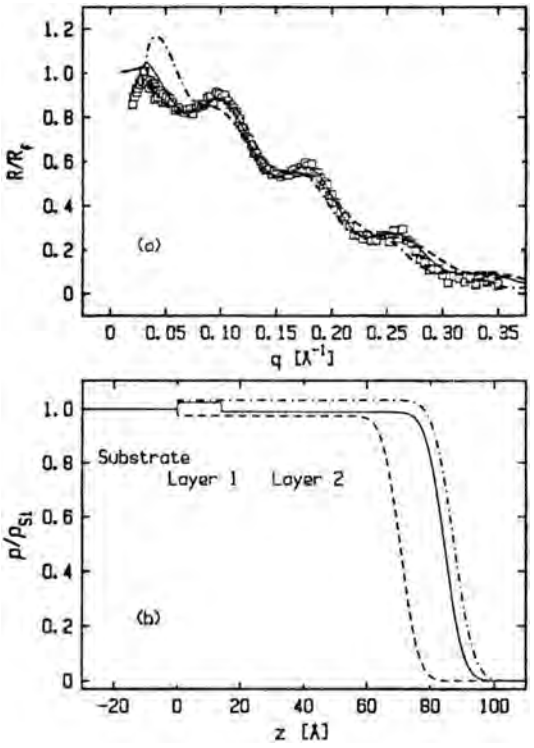


FIG. 24. Typical x-ray reflectivity data from an SiO_2 film (a), and fits corresponding to the real space models (b). In (b) the single oxide layer models (broken lines) produce poor fits, whereas the two layer model (solid line) fits the data well. Layer 1 is the higher density, interfacial SiO_2 layer [from Kosowsky *et al.* (Ref. 184)].

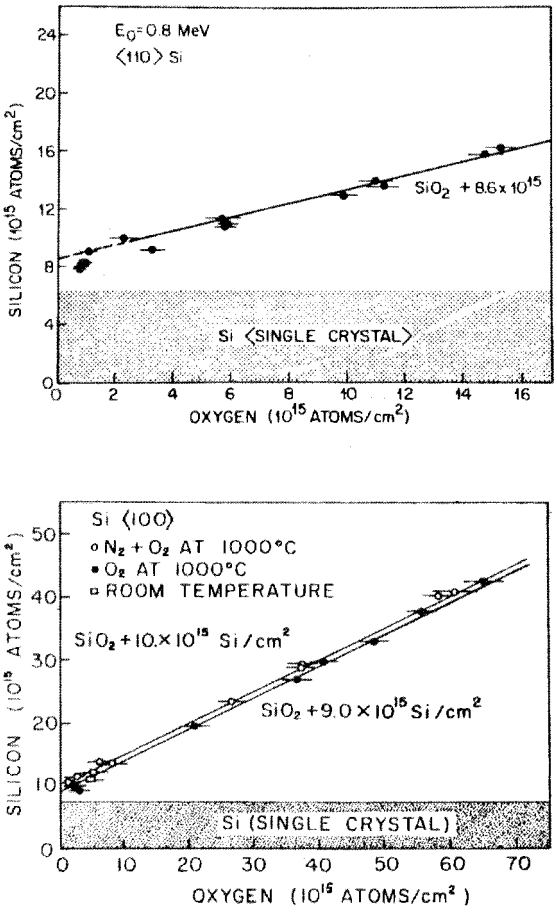


FIG. 26. Integrated amount of Si and O from Rutherford backscattering experiments for both the $Si(110)/SiO_2$ and $Si(100)/SiO_2$ systems [from Jackman *et al.* (Ref. 195)].

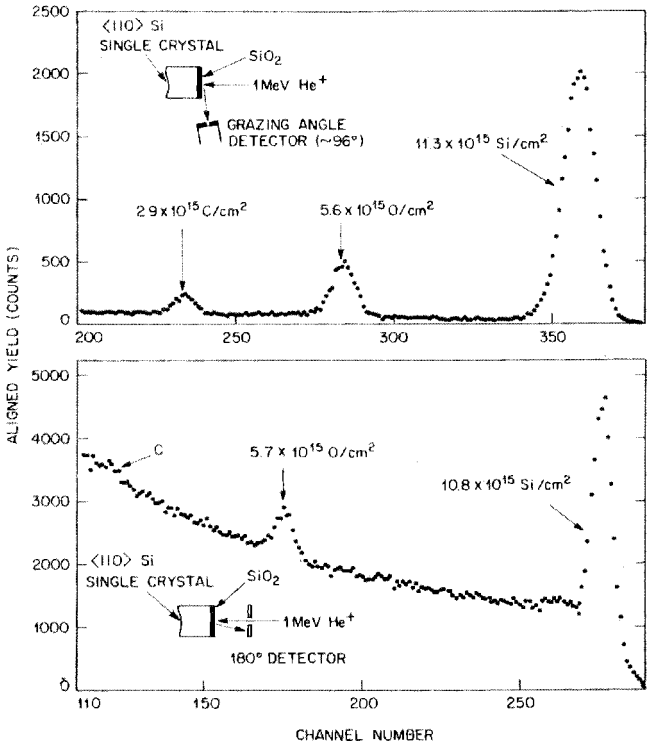


FIG. 25. Typical Rutherford backscattering energy spectra taken in a channeling configuration, with grazing exit angle (upper panel) and 180° backscattering (lower panel) detector geometries. The sample was Si(111) with ~1.5 nm of SiO_2 [from Jackman *et al.* (Ref. 195)].

can be improved by utilizing glancing angle geometries. Despite this shortcoming, it is important to know the integrated elemental concentrations in multicomponent films, and RBS is a very accurate technique for measuring film composition and stoichiometry, as well as impurity concentrations.

MEIS is based on the same ion–solid interaction principles as conventional RBS. A schematic of a typical MEIS experiment is illustrated in Fig. 27. Compared to RBS, MEIS uses lower ion beam energies, typically 100–200 keV. In this energy range, dE/dx, the stopping power, is at its maximum for protons or α particles in solids, resulting in optimal depth resolution. For example, the stopping power for ~100 keV protons is 130 eV/nm for Si, 120 eV/nm for SiO_2, 180 eV/nm for Ta_2O_5, and 200 eV/nm for Si_3N_4. More importantly, in MEIS backscattered ion energies can be measured with a high resolution toroidal electrostatic energy analyzer ($\Delta E/E \sim 0.15\%$, i.e., $\Delta E \sim 150$ eV for 100 keV ions), greatly increasing the energy resolution relative to the detectors used in conventional RBS. Taking into account the values of the stopping power and the travel length factor, this energy resolution translates into almost monolayer depth resolution in the near surface region. As an example, it has been demonstrated that 0.3–0.5 nm accuracy in N depth profiles, near the top surface or for ultrathin films, can be achieved,[201] as is illustrated in Fig. 28. However, due to the statistical nature of ion energy loss in solids, known as the straggling effect, the

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

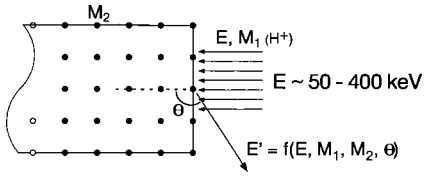


FIG. 27. Principles of a medium energy ion scattering experiment. MEIS is essentially a low energy, high resolution variant of Rutherford backscattering (RBS). E and E' are the incident and scattered particle (H^+) energies, M_1 and M_2 are the particle and target atomic masses, and θ is the scattering angle.

resolution decreases with increasing distance from the surface. We also note that a thorough understanding of straggling below the 2 nm range remains elusive.

MEIS allows one to simultaneously monitor absolute concentrations and depth profiles of N, O, Si, and other elements in dielectric films.[199–201,203,204,234–238] As in RBS, the detection limit is proportional to the square of the atomic number. Thus sensitivity is very high for heavy elements, but decreases with atomic number. For example, the detection limit of N in SiO_2 is $\sim 2\times 10^{14}$ N/cm^2, depending on film thickness and the width of the N distribution in the film. The detection of very light elements such as H and B can be enhanced in the elastic recoil configuration, as has been demonstrated,[198,239] Fig. 29. Light elements can also be detected in a forward scattering geometry, usually using a heavier element as the incident particle to increase the scattering cross section and to facilitate detection. This method is called elastic recoil detection (ERD),[240,241] or in the case of H detection, H forward scattering (HFS). Habraken and colleagues examined N, O, Si, and H using ERD of primary MeV ions.[37,225] More recently, Brijs[242] used a 60 MeV Ni beam, in a grazing angle geometry with a magnetic sector spectrometer, to look at forward scattering from ultrathin Si–O–N layers. An example of ERD to detect trace H in a Si_3N_4 film[241] is shown in Fig. 30.

It is worth noting that contrary to other depth profiling techniques such as SIMS, both the sensitivity to a given element in the film and the depth resolution increase with decreasing dielectric film thickness. Another strength of MEIS and most other ion scattering methods is mass sensitivity, which enables isotopic labeling experiments. The use of O isotopes (^{18}O and ^{16}O), in combination with high resolution depth profiling, has been used to study the mechanism of Si oxidation in the ultrathin regime.[199,200,204,238] The principle of such an ^{18}O labeling study is shown in Fig. 31. MEIS has also proven itself useful in the arsenal of tools used to analyze ultrathin high-κ metal oxides,[103,206–208] Fig. 32.

In addition to elastic scattering during ion–solid interactions (the bases of RBS and MEIS), high energy ions can induce nuclear reactions in the target.[25,216] NRA techniques are based on the detection of protons, α particles, and γ rays generated in nuclear reactions induced by the collision of high energy charged particles with N, O, Si, H, D, and other elements. Table V is a compilation of those nuclear reactions that have applicability for the study of dielectrics. The cross sections for these reactions can be determined in independent calibration experiments, and the signal-to-background ratio

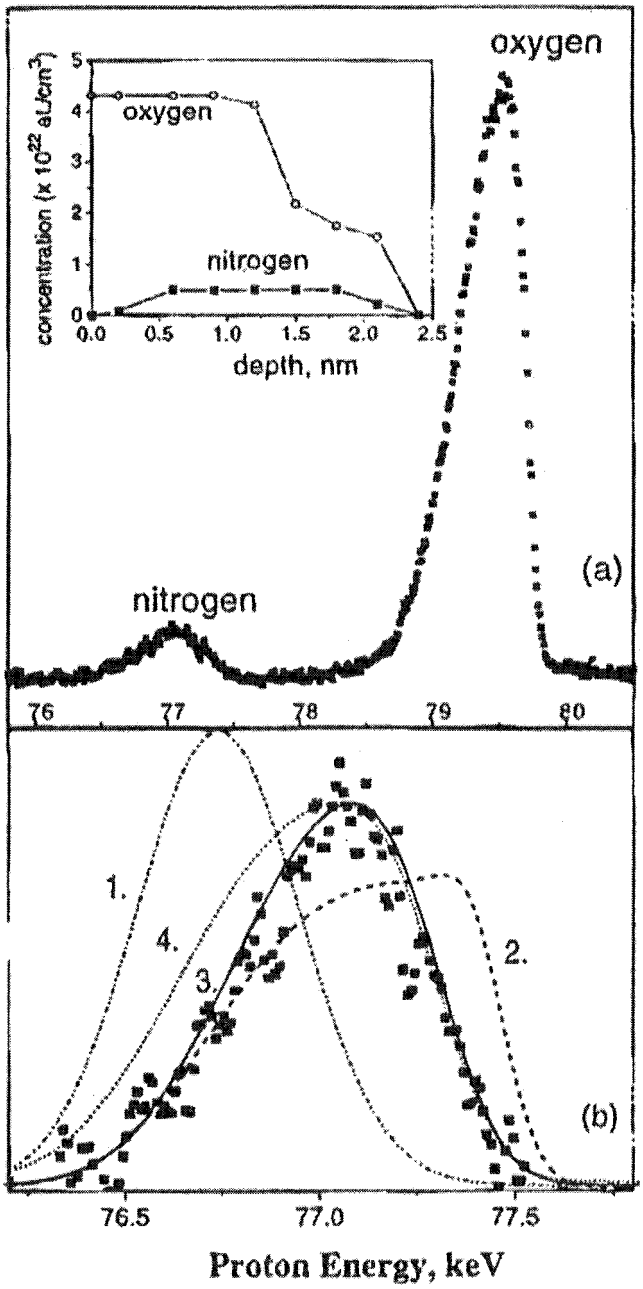


FIG. 28. A medium energy ion scattering study of a thin (~2 nm) Si–O–N film grown on Si(100) in a furnace at 950 °C for 60 min in NO ambient. The upper panel shows the scattering spectrum measured at a scattering angle of 125°. The inset shows the corresponding N and O profiles as a function of distance from the oxide surface. The lower panel shows a closeup of the spectrum in the N region along with the results of simulations for different N distributions: (1) all N (determined to be 8.8×10^{14} N/cm^2) is located at the Si/SiO_2 interface, (2) all N is uniformly distributed in the film, (3) N profile shown in the inset (best fit), and (4) N profile same as (3) but extended 0.3 nm into the substrate. Therefore profiles (1), (2), and (4) can be eliminated from consideration [from Lu *et al.* (Ref. 201)].

is in many cases quite favorable. Since the nuclear reaction rates are only sensitive to the number of nuclei in the films, the technique yields absolute concentrations of the species investigated. For example, the technique allows one to determine the absolute concentration of ^{14}N with 7%–10% accuracy at a detection limit of $\sim 5\times 10^{13}$ N/cm^2 via the reaction $^{14}\mathrm{N}(d,\alpha_{0,1})^{12}\mathrm{C}$, induced by 1.1 MeV deuterons.[173,243] The O

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

TABLE V. Compilation of useful nuclear reactions for gate dielectrics analysis.

Target element	Nuclear reaction	Energy, keV	Sensitivity, atoms/cm^2
H	$H(^{15}N,\alpha\gamma)^{12}C$	6420	$\sim 10^{14}$
D	$D(^3He,p)^4He$	700	$\sim 10^{12}$
^{14}N	$^{14}N(d,\alpha_{0,1})^{12}C$	1100	$\sim 5\times 10^{13}$
^{15}N	$^{15}N(p,\alpha)^{12}C$	1000	$\sim 10^{12}$
^{15}N	$^{15}N(p,\alpha\gamma)^{12}C$	429	$\sim 10^{13}$ (estimated)
^{16}O	$^{16}O(d,p)^{17}O$	850	$\sim 10^{14}$
^{18}O	$^{18}O(p,\alpha)^{15}N$	730	$\sim 10^{12}$
^{18}O	$^{18}O(p,\alpha)^{15}N$	151	$\sim 10^{13}$ (estimated)
^{27}Al	$^{27}Al(p,\gamma)^{28}Si$	405	$\sim 10^{13}$
^{28}Si	$^{28}Si(p,\gamma)^{29}P$	371	
^{29}Si	$^{29}Si(p,\gamma)^{30}P$	324 417	$\sim 10^{13}$ (estimated)
^{30}Si	$^{30}Si(p,\gamma)^{31}P$	499	$\sim 10^{13}$ (estimated)

content in films can also be measured by NRA, using the $^{16}O(d,p)^{17}O$ reaction at 850 keV.[212] Knowledge of these concentrations allows one to calculate film thickness, assuming that film density is known.[244] An additional advantage of the NRA technique is the detection of N(^{15}N) and O(^{18}O) isotopes with the help of the following reactions: $^{15}N(p,\alpha)^{12}C$ at 1000 keV, $^{18}O(p,\alpha)^{15}N$ at 730 keV, and the resonant reactions of $^{15}N(p,\alpha\gamma)^{12}C$ at 429 keV and $^{18}O(p,\alpha)^{15}N$ at 151 keV. An example of NRA analysis is shown in Fig. 33. Due to the narrow resonances of the latter two reactions, widths of 120 and 100 eV, respectively, they can be used for depth profiling of ^{15}N and ^{18}O on about a 1 nm depth scale, under favorable conditions.[219,245,246] Nitrogen depth profiling can also be performed by HF acid etch back and subsequent NRA measurement of N remaining in the film.[173] Isotopic labeling, in combination with NRA mea-

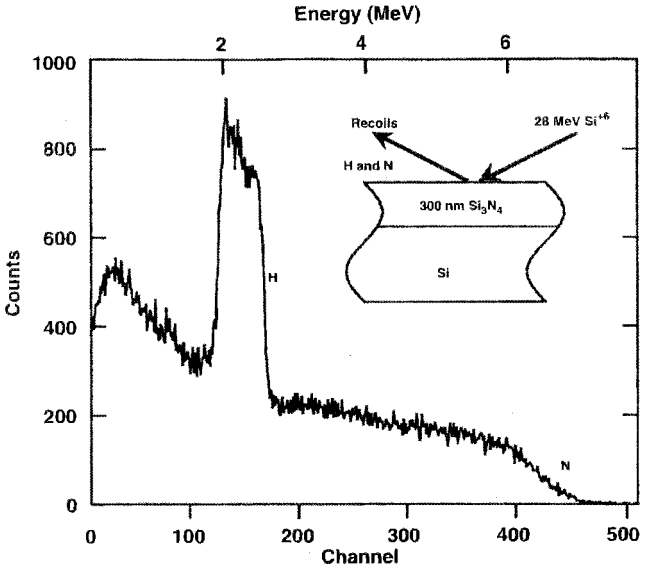
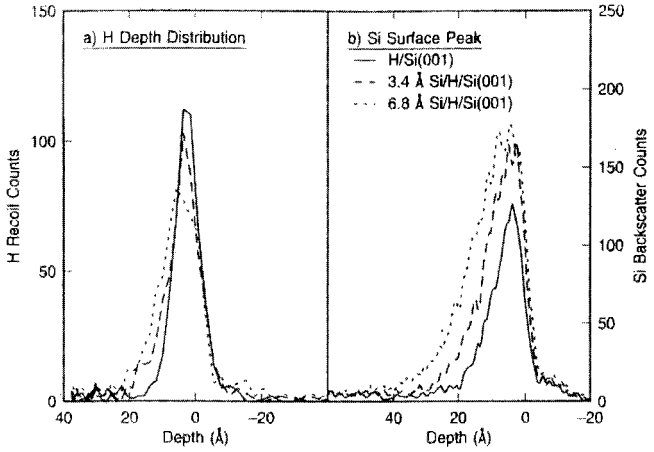


FIG. 30. An elastic recoil detection spectrum collected from a Si_3N_4 layer ~300 nm thick. A 28 MeV Si beam was used. The H is present as a minor constituent of the film, a remnant of chemical vapor deposition at 800 °C. The H signal is sitting on the N signal background [from Barbour *et al.* (Ref. 241)].



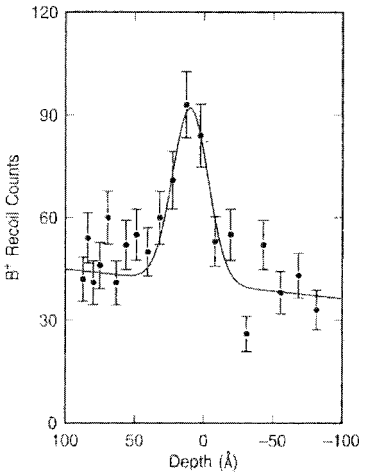


FIG. 29. Medium energy ion scattering elastic recoil spectra for a H terminated Si(100) surface followed by deposition of an ultrathin amorphous Si overlayer (upper panel), and B segregated to the Si(111) surface (lower panel) [from Copel *et al.* (Ref. 198)].

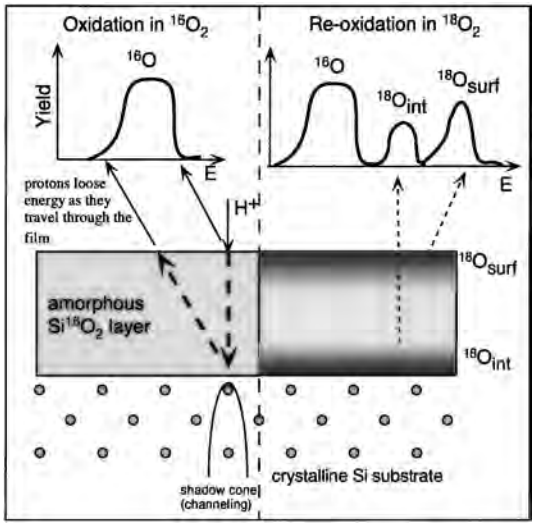


FIG. 31. Principles of an isotopic labeling (in this case $^{18}O_2$ reoxidation of an Si $^{16}O_2$ film) medium energy ion scattering experiment. ^{18}O is detected at the interface (new oxide growth) and at the oxide surface (surface exchange reaction).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

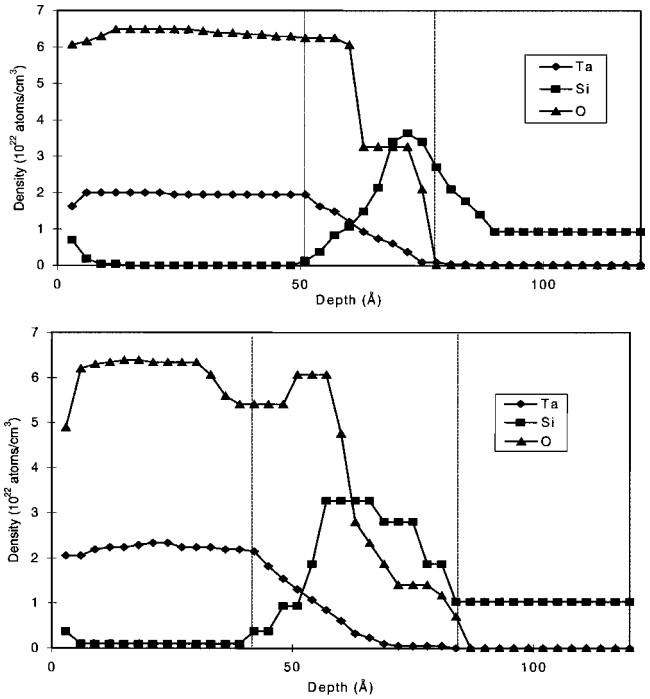


FIG. 32. Medium energy ion scattering depth profiles for a thin (7 nm) Ta_2O_5 film as-deposited on Si (upper panel) and after an ultrahigh vacuum anneal at 950 °C for 30 min (lower panel). The annealed sample shows significant intermixing near the interface [from Alers *et al.* (Ref. 103)].

surements, has proven useful for studying transport and incorporation of N and O during thermal oxynitridation in NO or N_2O.[25] A further useful application of NRA, Fig. 34, is based on its ability to detect H/D using the reactions $H(^{15}N,\alpha\gamma)^{12}C$ at 429 keV and $D(^3He,p)^4He$ at 700 keV, since H and D are believed to be important to device performance.[220,221,225,226]

SIMS is an industry standard technique, used to monitor concentration profiles in semiconductor structures. It has been used very effectively to study growth mechanisms of oxides,[228,230,247] as well as the incorporation of N[227,248] and H[231,249,250] in oxides. The SIMS experiment involves continuous sputtering of the sample and accurate measurement of the sputtered species by mass spectroscopy. Relative to RBS or MEIS, the technique has a very high sensitivity, on the order of 0.001 at. %, can be performed rapidly, and is more commonly available. However, the technique begins to reach its limiting depth resolution (estimated to be ~2 nm) for sub-5 nm films. Another more important complication of SIMS analysis is the matrix effect, in which the sputtered ion yield depends strongly on the local chemistry around the element. For example, in Si–O–N films, the ion yield of CsN^+ (Cs^+ being the sputtering ion) from N in bulk Si is about six times smaller than N in SiO_2. Further, the ion yield for N near the interface is about three times that observed in the bulk of an SiO_2 film.[227] This effect is shown in Fig. 35. The use of CsN^+ ions as the detected species seems to minimize the matrix effect, since for negative ions matrix effects are even more severe. In many cases, SIMS analysis is also complicated by surface contamination and initial sputtering effects, which make quantitative measurements of the com-

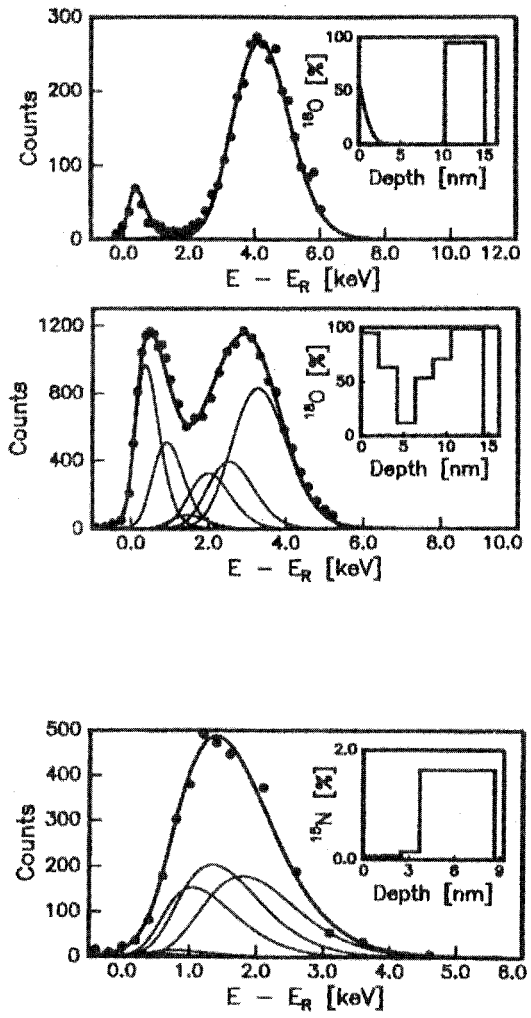


FIG. 33. Isotopic labeling during N_2O oxynitridation of Si, studied in combination with nuclear reaction analysis. Excitation curves are shown for the nuclear reaction $^{18}O(p,\alpha)^{15}N$, for SiO_2 reoxidized in $^{18}O_2$ (top), and Si oxynitrided in N_2O and reoxidized in $^{18}O_2$ (middle). ^{18}O depth profiles are shown in the insets. The bottom figure is the excitation curve of the nuclear reaction $^{15}N(p,\alpha\gamma)^{12}C$ for a Si–O–N film obtained by thermal annealing of SiO_2 in $^{15}N_2O$. The inset shows the ^{15}N depth profile [from Ganem *et al.* (Ref. 217)].

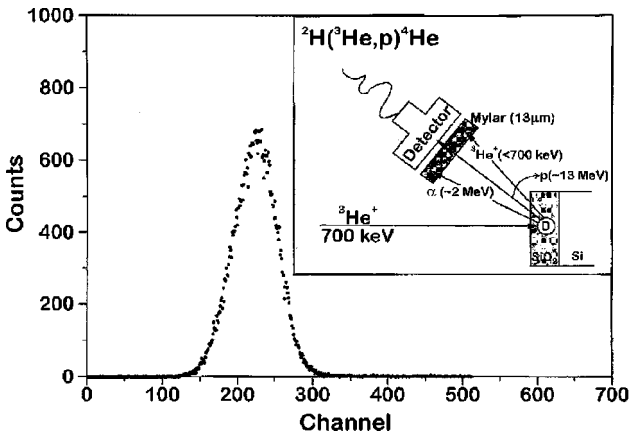


FIG. 34. Nuclear reaction analysis detection scheme and a typical spectrum for D in SiO_2 films [from Baumvol *et al.* (Ref. 220)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

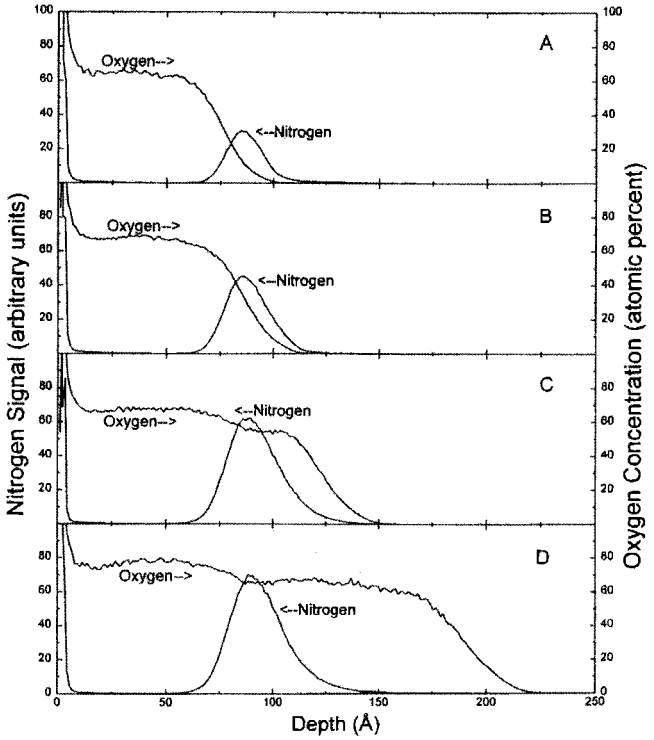


FIG. 35. Illustration of the matrix effect in N secondary ion mass spectroscopy analysis. SIMS profiles shown in B, C, and D correspond to the film shown in A, but reoxidized in O_2 for different times. One can see how the area under the N peak increases as the N is pushed away from the Si/SiO_2 interface, even though the amount of N in the film remains constant [from Frost *et al.* (Ref. 227)].

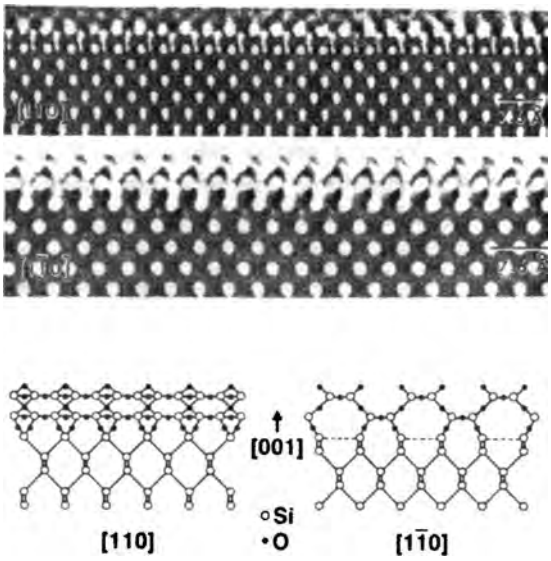


FIG. 36. Transmission electron microscopy lattice images of the $Si(100)/SiO_2$ interface in two orthogonal ⟨110⟩ projections. Interface sharpness and flatness, as well as the presence of a new interfacial structure were stressed in the original paper. A schematic representation of the proposed interface structure is also shown [from Ourmazd *et al.* (Ref. 749)].

position near the top ~1 nm surface layers difficult. However, high depth resolution SIMS analysis has proven very useful for investigating ultrathin Si–O–N films.[248] One more aspect of SIMS analysis is that the peak concentration of an element, and details of its profile in ultrathin films, may not be accurate, due to ion mixing. The measured areal density of the element should be used instead. Reference samples calibrated by other quantitative methods (NRA, MEIS, etc.) allow for more accurate SIMS analysis.

Finally, we mention one more high energy technique, positron spectroscopy,[251–253] that has potential for the study of defects in MOS structures. Based on the transport and annihilation of positrons in voids in solids, results have demonstrated a correlation between positron annihilation data and the generation rate of interface states.[252,253]

D. Electron microscopy

Electron microscopy, either in transmission (TEM) or scanning reflection (SREM) modes, is a powerful technique for visualizing the structural and morphological features of semiconductors.[254–256] An excellent example of its application to the study of the Si/SiO_2 interface is shown in Fig. 36. Initially, TEM was used as a direct way to measure oxide thickness and film roughness.[108,257–259] However, for SiO_2 films thinner than ~2 nm the use of TEM to measure oxide thickness becomes problematic due to uncertainty in defining the Si/SiO_2 and polycrystalline Si/SiO_2 interfaces, since the image is averaged over the travel length of electrons in the sample.[40] Over the past decade, electron microscopy has advanced in sophistication along two main directions: atomic resolution imaging[17,255,260–265] and real-time observation of processes such as oxidation.[254,266–271] Further, atomic column scanning in TEM has been made possible by generating very small (~0.2 nm) electron probes.[17,261–263,265] Using such probes, atomic number (Z) contrast structure imaging[265] and electron energy loss spectroscopy (EELS)[17,261,263] can be performed. A schematic diagram of an atomic probe microscopy apparatus with EELS is shown in Fig. 37. The Z-contrast method allows one to obtain direct information about atomic positions, since scattering power varies with atomic number. In EELS, a fraction of the transmitted electrons lose energy by exciting a target atom's core electrons, and are thus characteristic for that atomic species, as well as its chemical state. EELS can therefore probe variations of composition as a function of distance from the interface, even for amorphous materials (see Fig. 6).

Real-time measurement capabilities are *de rigueur* for studies of dynamic processes. TEM[266–268] and SREM[254,270,271] have been used to understand the details of Si oxidation and etching (from SiO desorption at elevated temperatures). Real-time studies of the interaction of O with the Si(111) surface as a function of temperature, pressure, and time have been performed.[266–268] A layer-by-layer oxide growth mode, illustrated in Fig. 38, was clearly observed at high pressure and low temperature. At high temperature and low pressure, the SiO desorption regime, step flow was observed. The intermediate regime was characterized by surface roughening. Layer-by-layer oxidation of Si(001) was also observed by SREM,[270,271] a technique illustrated in Fig. 39. The initial stages of Si oxidation,[272] Fig. 40, as well as nitridation[273] have also been studied by low energy electron microscopy (LEEM).[274]

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

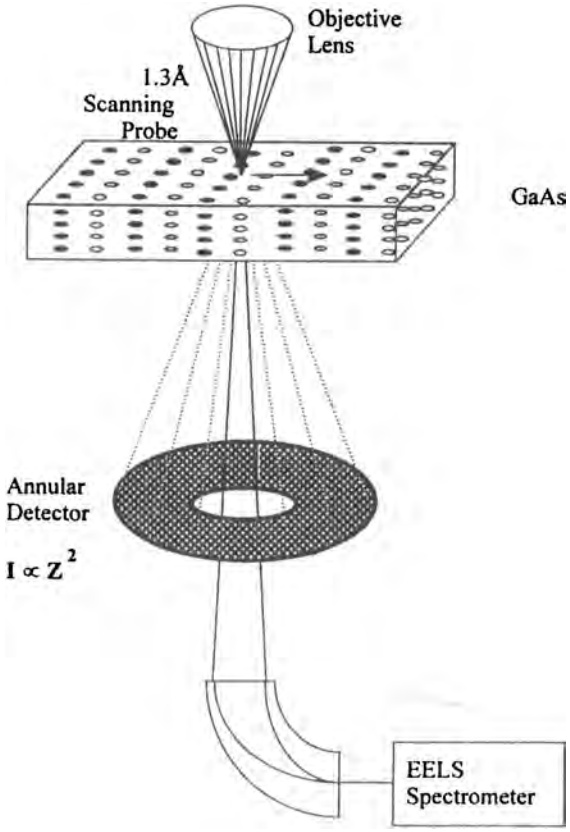


FIG. 37. Schematic illustration of a high resolution transmission electron microscopy, electron energy loss spectroscopy experiment [from Duscher *et al.* (Ref. 265)].

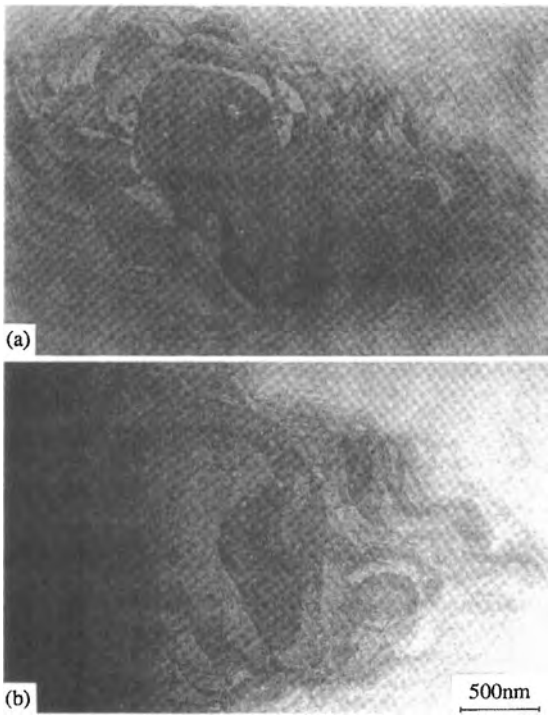


FIG. 38. Transmission electron microscopy images (a) of a clean Si(111)(7×7) surface and (b) the same area after exposure to 1 atm of O_2 at 400 °C for 20 min (oxide thickness ~1.0–1.5 nm). One can see the identical step distribution in the two images [from Ross *et al.* (Ref. 268)].

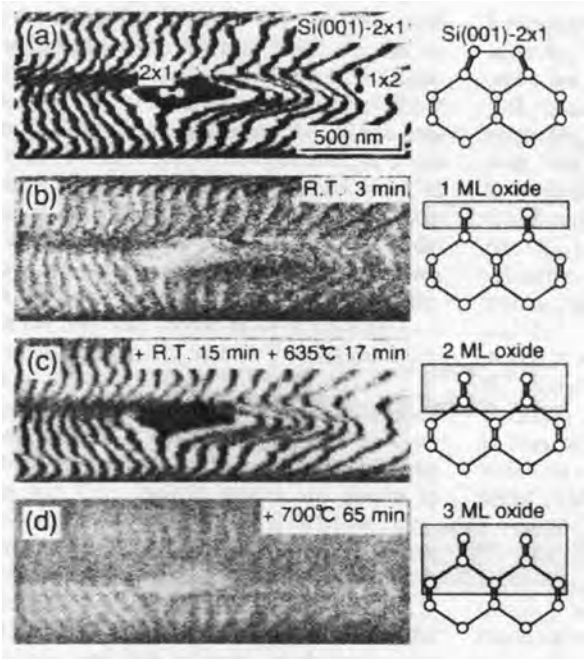


FIG. 39. Scanning reflection electron microscopy images of Si(100) surfaces before (a), and after the oxidation times and temperatures shown (RT =room temperature). The first contrast reversal (b) corresponds to oxidation of the uppermost dangling bonds and the first subsurface layer. The following images (c) and (d) correspond to second and third layer oxidation [from Watanabe *et al.* (Ref. 271)].

E. Scanning probe microscopy

Scanning probe microscopy techniques such as atomic force microscopy (AFM) and scanning tunneling microscopy (STM) are important methods for imaging the surface morphology of ultrathin dielectric films. Since the invention of STM almost 20 years ago,[275–277] probe microscopy methods have been successfully applied to study surface structure,[278,279] interfacial roughness,[280,281] wafer surface morphology after various pregate oxidation cleaning steps,[282,283] initial stages of Si oxidation,[284–292] initial stages of nitridation,[160,273,293–299] and oxide decomposition.[300,301] An example of the applicability of STM is shown in Fig. 41. Spectroscopic mode STM experiments were used to study oxide breakdown mechanisms, and also to identify O bonding configurations during initial oxidation.[302] A fundamental limitation of probe microscopy methods is related to the probe tip size and shape.[303] STM usually affords the best lateral and vertical resolution. Since the radius of the tip is typically on the order of ~10 nm, it is difficult to observe smaller features, e.g., short wavelength roughness, especially if they have a high aspect ratio. In general, the lateral resolution is better for STM than AFM, in part because in AFM the tip tends to broaden due to contact with the sample. A fundamental limitation for STM as it applies to SiO_2-based dielectrics is the large band gap of SiO_2 (~9 eV), which usually limits STM studies to films less than ~1.5 nm thick. Alternate (high-κ) dielectrics have smaller band gaps and are often O deficient, resulting in energy gap states. These properties result in a higher conductivity (at a given voltage and equivalent thickness), than SiO_2, enabling the use of STM for the examination of thicker, high κ dielectric films.

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

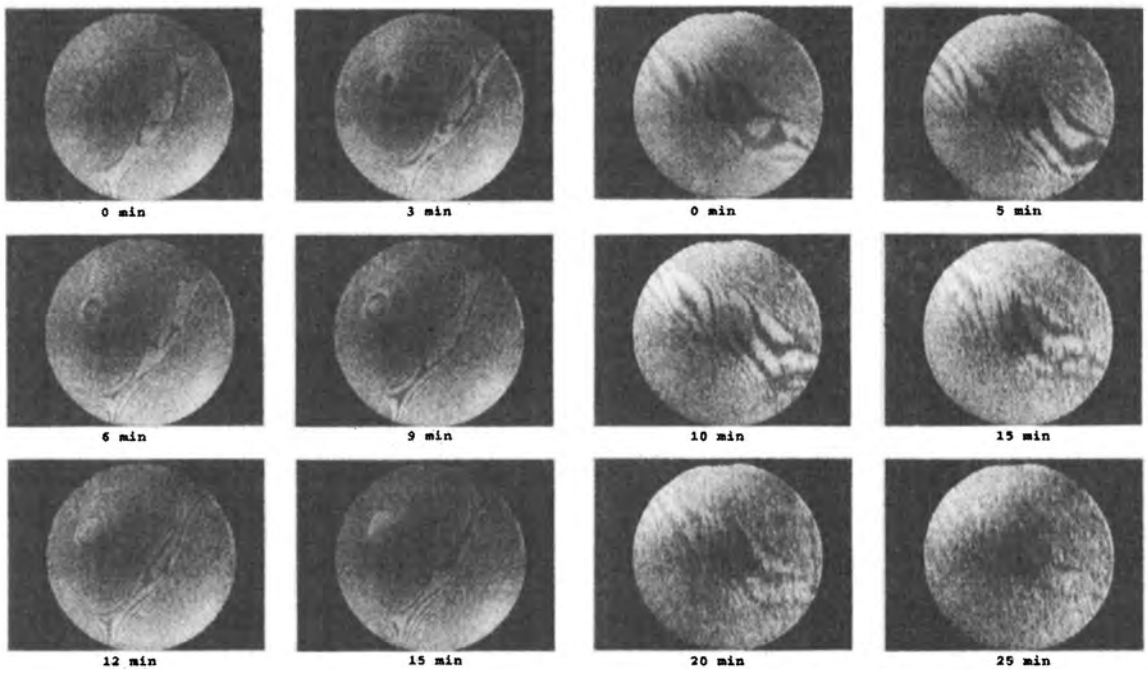


FIG. 40. Low energy electron microscopy video images of the Si(100)-(2×1) surface exposed to 5×10^{8} Torr of O_2 at 600 °C (left) and 550 °C (right), as a function of O_2 exposure time. One can clearly see a transition from a step flow etching mode (left) to a random terrace etching regime. [From Wurm *et al.* (Ref. 272)].

Ballistic electron emission microscopy (BEEM),[304,305] scanning microwave microscopy (SMM),[306–309] scanning capacitance microscopy (SCM),[310] scanning tunneling spectroscopy (STS),[311,312] and hot electron emission microscopy (HEEM)[313] are recent variations of scanning probe techniques for the study of thin dielectric films. The BEEM technique, shown in Fig. 42, is based on the local ballistic transport of electrons emitted from an STM tip through a thin metal electrode/thin oxide/Si structure.[305] It has been used to better understand the mechanism of defect generation in thin oxides, and therefore oxide breakdown. In HEEM, hot electrons emitted into vacuum from biased MOS structures form a direct image of spatial emission distribution and can be used to investigate prebreakdown phenomena with less than 20 nm spatial resolution. SMM measures the response of a thin dielectric film to a microwave cavity scan.[306–308] It allows one to measure the dielectric constant of the film, making the technique especially attractive for high κ studies, as is shown in Fig. 43. However, poor lateral resolution ($\sim$1 μm) precludes its use for studying small features. SCM has recently been used to study the gate region of ultralarge scale integration (ULSI) transistors, but its low lateral resolution limits its ability to image the gate.[314,315] SCM allows one to image the tunneling current through an oxide at a given bias, while simultaneously recording the AFM image.

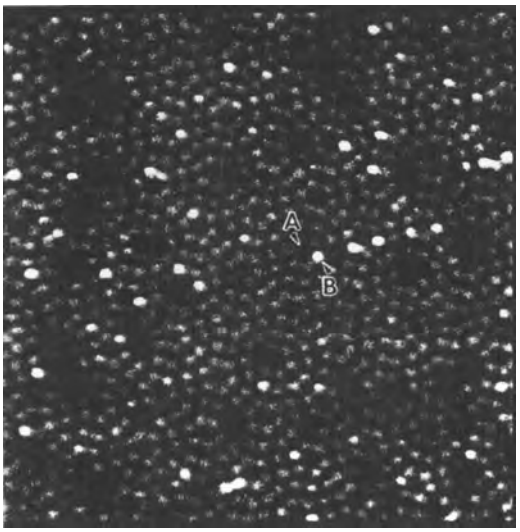


FIG. 41. Atomic resolution scanning tunneling microscopy image of the unoccupied states of a Si(111)-7×7 surface exposed to a small amount of O_2 (0.2 L) at room temperature. At least two different configurations of O (bright and dark spots A and B) are seen [from Avouris *et al.* (Ref. 285)].

III. ELECTRICAL CHARACTERIZATION METHODS AND PROPERTIES

In this section we will discuss the electric characterization of ultrathin oxide layers. As the thickness is scaled from 4 to 1 nm, an increasing complexity in the interpretation of electrical data is observed. We will show that capacitance–voltage ($C-V$) measurements require quantum mechanical corrections, gate leakage current is dominated by direct, rather than Fowler–Nordheim tunneling, and charge pumping measurements need corrections for excessive leakage current. When electrically stressed, the basic oxide degradation mechanisms described for thicker oxides ($t_{ox}>4$ nm) are still applicable. Oxide wearout can be described as the continuous creation of trapping centers. These traps cause stress-induced leakage current, and can trap charge until breakdown is finally triggered. The occurrence of soft breakdown

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

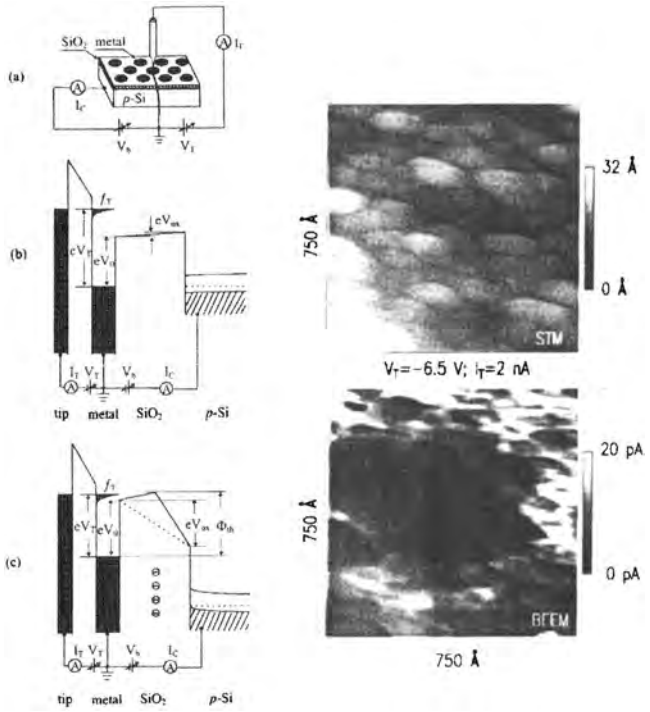


FIG. 42. Schematic of a ballistic electron emission microscopy experiment on a MOS structure, including (a) layout of the experiment, (b) band structure for $V_b=0$, and (c) for $V_b>0$. Images shown on the right correspond to a 4 nm Pd/7. 1 nm SiO_2/p-Si capacitor structure [from Ludeke *et al.* (Ref. 305)].

in ultrathin oxide layers impacts their reliability and also changes the breakdown detection technique. Despite all the missing links in our understanding of the electrical properties of ultrathin SiO_2 layers, a quite complete picture of the essential physical phenomena is in place.

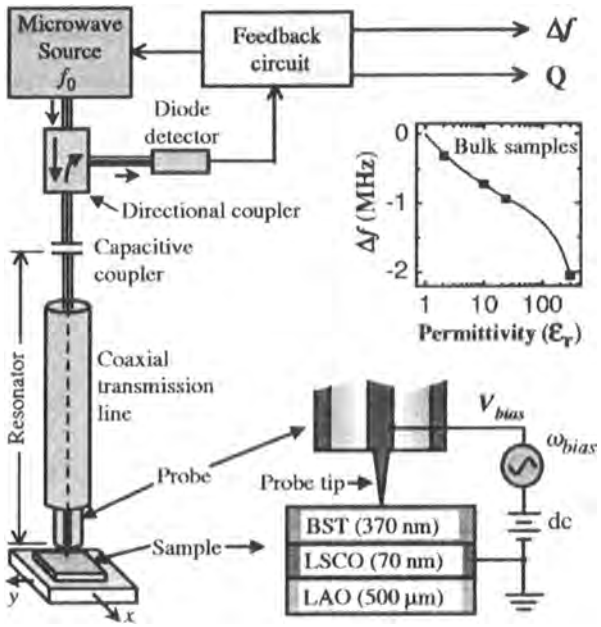


FIG. 43. Schematic of the near-field scanning microwave microscope. The graph inset shows measured (points) and modeled (line) permittivity results for samples of different permittivities [from Steinhauer *et al.* (Ref. 308)].

A. Characterization methods

In this section, the application of electrical characterization techniques to sub-4 nm oxides will be discussed. We will focus on the three most commonly used measurements: $C-V$, leakage current, and charge pumping (CP).

1. C–V measurements

The most frequently used electrical technique to assess the properties of both the thin oxide layer and its interface with Si is the $C-V$ measurement. In thicker oxide layers $C-V$ curves can be fitted satisfactorily with classical models, described in textbooks.[316] The $C-V$ technique can be used to determine flatband and threshold voltage, fixed charge, and interface state density. It is also often used to determine the oxide thickness.

In sub-4 nm oxide layers, $C-V$ measurements provide the same information, but the interpretation of the data requires considerable caution. The assumptions needed to construct the ''classical model'' are no longer valid, and quantum mechanical corrections become mandatory, thus increasing the complexity of the analytical treatment. First, several authors have demonstrated that for ultrathin layers, Maxwell–Boltzman statistics no longer describe the charge density in the inversion and accumulation layers satisfactorily, and should be replaced by Fermi–Dirac statistics.[317,318] In addition, band bending in the inversion layer near the semiconductor–insulator interface becomes very strong, and a potential well is formed by the interface barrier and the electrostatic potential in the semiconductor. This potential well may be narrow enough to give rise to electron confinement at discrete energy levels,[317–319] as illustrated in Fig. 44(a). The correct analytical treatment requires solving the coupled effective mass Schrodinger and Poisson equations self-consistently.[318] Closed form analytical treatments require a simplification of the problem,[320,321] e.g., replacing the actual potential well by a triangular well and/or by considering only the lowest subbands. One of the main effects of the quantum mechanical treatment of the inversion layer is a considerable shift of the inversion charge centroid away from the semiconductor–insulator interface, as illustrated in Fig. 44(b). This effect can be modeled as an additional capacitor in series with the oxide capacitance.

A similar effect is generated by polycrystalline Si depletion on the gate side of the capacitor of a MOS transistor.[318,322] This effect is related to both the high fields at the insulator surface as well as the incomplete activation of the dopants near the polycrystalline Si/SiO_2 interface. A carrier concentration profile with a finite width, having a centroid several tenths of a nanometer away from this interface, results. This effect can also be modeled as an additional capacitance in series with the oxide capacitance. As a consequence of quantum mechanical effects and polycrystalline Si depletion, the measured capacitance is smaller than the expected (physical) oxide capacitance, and the difference becomes very significant for ultrathin layers. This also implies that oxide thickness extraction from $C-V$ measurements becomes more difficult, but not impossible. If $C-V$ curves are fitted properly, a good agreement between $C-V$ extracted

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

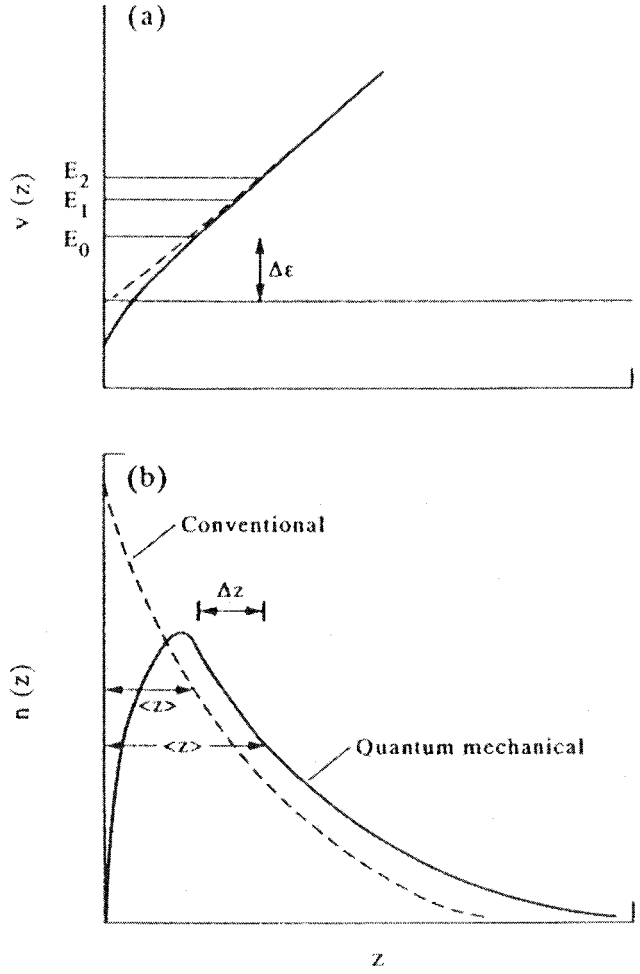


FIG. 44. (a) Schematic representation of a potential well in strong inversion. In the state of weak inversion the triangular shape is adequate. In the quantum mechanical picture the energy spectrum consists of a discrete set of energy levels. The first energy level does not coincide with the bottom of the conduction band. (b) Electron density as a function of distance from the interface. The average distance to the interface is larger in the quantum mechanical framework. Therefore a larger band bending is needed for a given population in the conduction band [from Van Dort *et al.* (Ref. 319)].

oxide thickness and physical oxide thickness, measured by ellipsometry, for example, may be obtained, as illustrated in Figs. 10 and 45.[60,108,317,318,320]

For very thin oxides (typically sub-2 nm), the huge leakage current through the oxide, due to direct tunneling of electrons (see Sec. III A 2 and Fig. 5), creates an additional complication in the interpretation of $C-V$ curves. A sharp drop in the capacitance is observed as the voltage increases.[321,323,324] This effect is illustrated in Fig. 46 and can be modeled by taking into account the tunnel conductance and an additional series resistance.

2. Gate tunnel current

When a voltage, V_{ox}, is applied across an oxide layer with thickness t_{ox}, the resulting oxide field, $E_{ox}=V_{ox}/t_{ox}$, gives rise to a current flow through the oxide. This current originates from electrons that quantum mechanically tunnel through the Si/SiO_2 potential barrier from the Si conduction band to the SiO_2 conduction band, as is illustrated in Fig. 47. When the tunneling occurs through a triangular barrier, Fig.

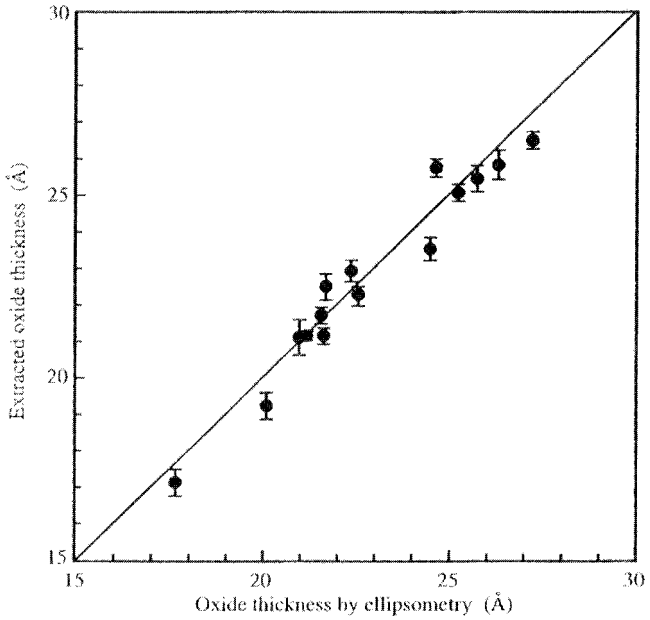


FIG. 45. Comparison between capacitance–voltage extracted oxide thickness and thickness measured by ellipsometry. Every ellipsometric thickness represents the average of nine points and every $C-V$ extracted thickness represents the average of 64 capacitors (area 10^{-4} cm^2) over a 200 mm wafer. The $C-V$ extracted thickness obtained using quantum mechanical models agrees well with the ellipsometric thickness [from Lo *et al.* (Ref. 318)].

47 (left), the conduction mode is called Fowler–Nordheim (FN) tunneling[325] and the measured current density, J_{FN}, can be described by the well-known formula:

$$J_{FN}=A\cdot E_{ox}^2\exp\left(\frac{-B}{E_{ox}}\right). \tag{3}$$

A and B are two constants, and B is related to the electron effective mass in the oxide conduction band and the Si/SiO_2 barrier height. In thin oxide layers, oscillations in the gate

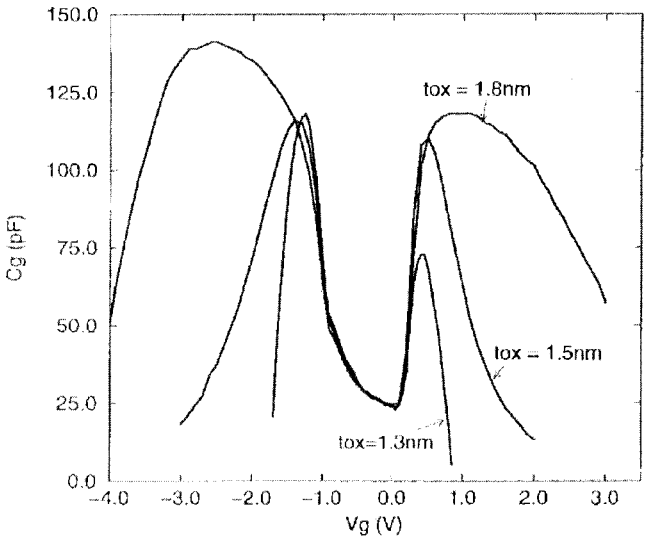


FIG. 46. Experimental metal–oxide–semiconductor capacitance–voltage curves for 1.3, 1.5, and 1.8 nm SiO_2 films, respectively. The sharp decrease of the gate capacitance results from high gate tunneling current [from Choi *et al.* (Ref. 321)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

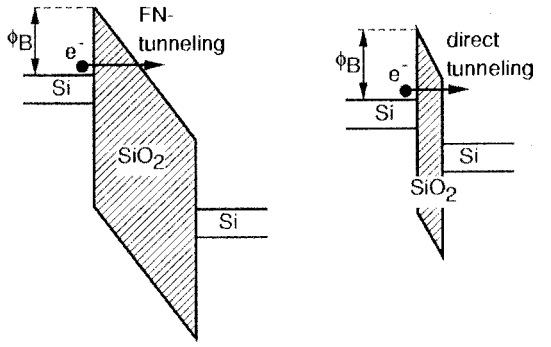


FIG. 47. Schematic illustration of Fowler–Nordheim (left) and direct (right) tunneling mechanisms of electron flow though an oxide potential barrier of height Φ_B.

current occur. These arise from the interference of incident and partially reflected electron waves propagating between the conduction band edge and the anode interface.[326–328]

When the oxide voltage drops below 3.7 V, electrons no longer enter the oxide conduction band, but tunnel directly from the anode to the cathode, as illustrated in Fig. 47 (right). In state-of-the-art CMOS technologies, direct tunneling is the dominant current conduction mechanism at operating voltage, and for oxide layers less than ~3 nm it is also the conduction mode for accelerated oxide wearout and breakdown tests. The direct tunneling current density cannot be described easily in a closed analytical form, but several approximate formulas and computer simulations can be found in the literature.[48,329–333] The general trend in these analytical formulas is that precision is bought at the expense of complexity. The simplest analytical expressions fail in the low voltage range, the very range of interest to forecast the leakage current at operating voltage. In Fig. 48, the I_G-V_G characteristics for oxides between 9.7 and 2.2 nm thick are shown. The change from a FN tunneling to a direct tunneling mechanism is indicated. The huge increase due to direct tunneling, as shown in Fig. 5, poses a major leakage current problem in VLSI technologies and severely limits the scaling of the oxide thickness.

A special case arises when a p^+ polycrystalline Si/oxide/Si structure is biased with negative gate voltage. Since the inversion layer cannot form in the highly doped p^+ polycrystalline Si, electrons are injected from the valence band. This is evidenced by the higher potential barrier extracted from the I_G-V_G characteristic, as well as by experiments using a polycrystalline SiGe electrode.[334–336] Charge separation experiments demonstrated that in this case, for ultrathin oxides at low voltage, hole tunneling from the anode dominates the gate current.[337]

3. Charge pumping

Charge pumping is a technique well suited to electrically characterize the Si/SiO_2 interface, and it has been used to study both interface quality and subsequent degradation under electrical stress.[338,339] Charge pumping consists of measuring the dc current at the Si substrate, due to recombination processes at interface defects, while pulsing the interface from accumulation to inversion under the action of periodic

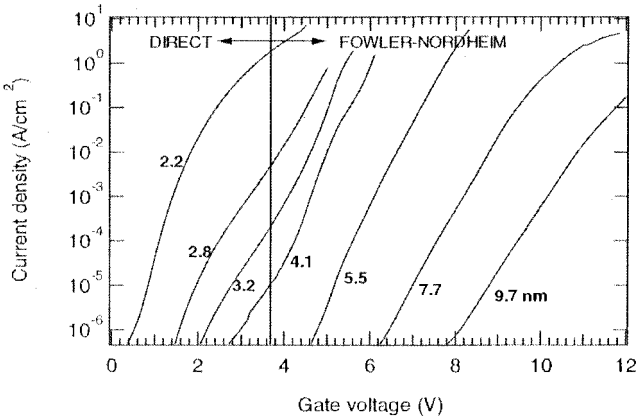


FIG. 48. The gate current density as a function of gate voltage for SiO_2 films with thicknesses between 2.2 and 9.7 nm. The transition from Fowler–Nordheim to direct tunneling is indicated [from Degraeve *et al.* (Ref. 3)].

gate pulses. When ultrathin oxide layers are investigated, a parasitic current component, resulting from direct electron tunneling, is added to the charge pumping current, as illustrated in Fig. 49.[340] This effect is very similar to that observed in $C-V$ measurements (see Fig. 46) and can lead to large errors in the extracted interface trap density and the flatband and threshold voltages. However, since the charge pumping current is proportional to the measurement frequency, whereas the leakage current is not, the charge pumping signal can be easily extracted by combining low and high frequency measurements.[340] Consequently, charge pumping remains a simple and accurate method that allows the determination of interface trap density, without the quantum mechanical modeling required for $C-V$ measurements.

B. Oxide degradation during electrical stress

In this section oxide degradation during electrical stress, ultimately leading to breakdown, is discussed. We define oxide degradation as the continuous, gradual deterioration of the oxide properties, resulting from structural damage generated in the oxide by electrical stress. Breakdown is triggered when the accumulated damage reaches a critical level. Dur-

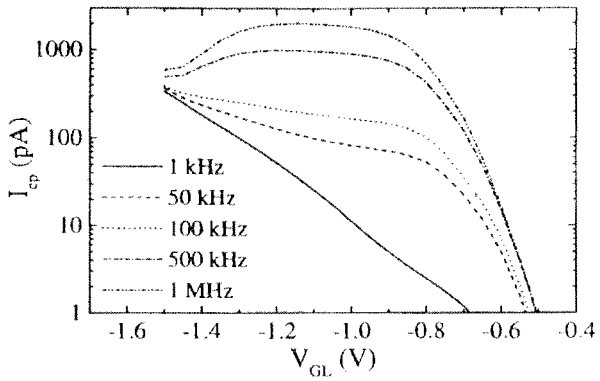


FIG. 49. Frequency dependence of the charge pumping current vs gate pulse base level on a 10×3 mm^2 N-channel transistor having 1.8 nm gate oxide. Measurement conditions: sinusoidal gate pulses, 2 V pulse amplitude, 0 V reverse bias. The charge pumping signal is superimposed on the gate oxide leakage current [from Masson *et al.* (Ref. 340)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

ing oxide stressing, several properties can be monitored, such as interface trap creation, negative and/or positive charge trapping, hole fluence, neutral electron trap creation, and the generation of a stress-induced leakage current (SILC). These properties are important indicators of oxide stress and can help one understand degradation mechanisms.

Several research groups have proposed breakdown models that directly correlate one of these properties with breakdown. One line of thought is common to all models: some damage related parameter exceeds a critical threshold at the moment breakdown is triggered. An important observation is that a relationship between accumulated oxide damage and breakdown is only found for intrinsic breakdown. Extrinsic breakdown is determined by localized, defect related physical processes that do not influence global degradation phenomena.

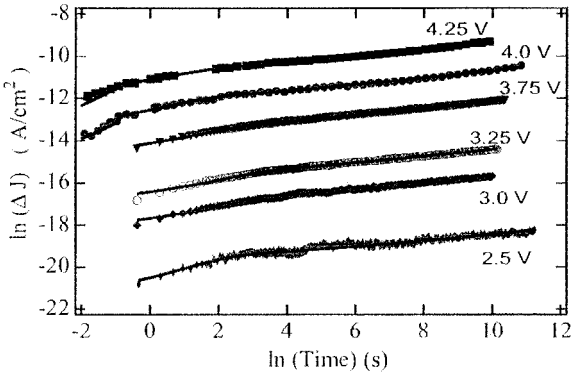


FIG. 50. Increase in current as a function of stress time for different gate voltages. Solid lines are fit assuming a single trap mechanism plus stress induced leakage current [from Nigam *et al.* (Ref. 347)].

1. Interface trap creation

During high field oxide stressing, interface traps are created at the Si/SiO_2 interface.[341,342] Their density can be obtained either from $C-V$[316] or charge-pumping measurements on transistors.[338] Recently, low voltage SILC measurements on sub-3.5 nm oxides have been used to quantify the interface trap density.[343] The mechanisms proposed for interface trap generation correspond to those for bulk trap generation, and will be discussed later in this section.

It has been claimed that the interface trap density, D_{it}, reaches a critical density, $D_{\mathrm{it,crit}}$, at the moment of oxide breakdown. In earlier work, the triggering of breakdown was thought to be caused by a local interface softening due to trap accumulation,[341] but more recently the critical interface trap density is merely viewed as a monitor for the total density of traps in the oxide. By means of a percolation model[55,344,345] (to be discussed in detail later), the interface trap density can be related to this total density.[56]

2. Oxide charge trapping

In oxides of thickness greater than 4 nm, a typical observation during high field constant current stressing (CCS) is the initial decrease of the applied voltage needed to achieve the required current, followed by a voltage increase which can become larger than the initially applied voltage.[341,346] The voltage shifts are caused by charge trapping of initially positive then negative charges, leading to oxide field distortion and subsequent change in the tunnel current density. During constant voltage stressing (CVS), exactly the opposite current shifts are measured, i.e., an initial increase of the current followed by a decrease.

In sub-4 nm oxides the charge buildup almost completely disappears. Typically, as illustrated in Fig. 50, a very small increase of the stress current during CVS is measured, which is attributed to positive charge trapping and the gradual generation of a SILC.[347] In some previous work[348,349] it was claimed that positive charge trapping in the oxide was responsible for triggering the breakdown event. During CCS, for example, locally enhanced charge trapping will not influence the total current density in the capacitor; however, it may lead to a local current density increase, resulting in an increased stress, which in turn leads to further positive charge trapping. In this way, a positive feedback mechanism is initiated that finally results in breakdown. Two arguments oppose this idea: (i) in ultrathin sub-4 nm oxides the measurable positive charge trapping is extremely small and yet the oxides break down, and (ii) the possible role of the negative charge in the oxide is completely ignored, while for $t_{\mathrm{ox}}>4$ nm the net charge trapped at breakdown is negative. Other work[350–352] claims that the net negative trapped charge in the oxide exceeds a critical threshold value at breakdown. Vincent *et al.*[352] related their observation to charge trapping kinetics, without assuming any additional trap creation. This is in contradiction with most work on oxide degradation that clearly show an increase in the trap density.

3. Hole fluence

When the gate oxide of an NMOSFET is stressed with a positive gate voltage, while source and drain are grounded, electrons tunneling through the oxide are provided from the source and drain and injected from the transistor channel. In this configuration, a positive current can be measured at the substrate (charge separation technique).[349,353] The substrate current density has a similar oxide field dependence as the FN current density, as is shown in Fig. 51. However, it should be noted that the curves in Fig. 51 are not parallel; the ratio between gate and substrate current depends on the oxide field. A well-known and widely accepted explanation for the physical origin of the substrate current has been given,[354–356] and is schematically illustrated in Fig. 52. When the injected electrons enter the anode (the polycrystalline Si gate), they lose their energy by creating high energy holes, possibly through the excitation of some intermediate state,[357] and these holes can then be injected back into the oxide. The hole fluence reaches the cathode and is measured as a positive substrate current, J_p. In ultrathin oxide layers the valence band injection of electrons can generate a hole current that may dominate the anode hole-generated current.[356]

Another possible explanation for the substrate current is the creation of holes in the cathode by photons generated in the anode. This has been suggested by DiMaria *et al.*,[358] and

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

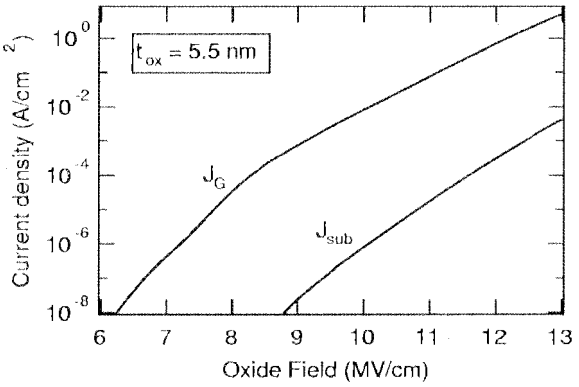


FIG. 51. Gate and substrate currents as a function of oxide field in a carrier separation experiment. The ratio J_{sub}/J_g is field dependent, increasing with increasing field [from Degraeve *et al.* (Ref. 3)].

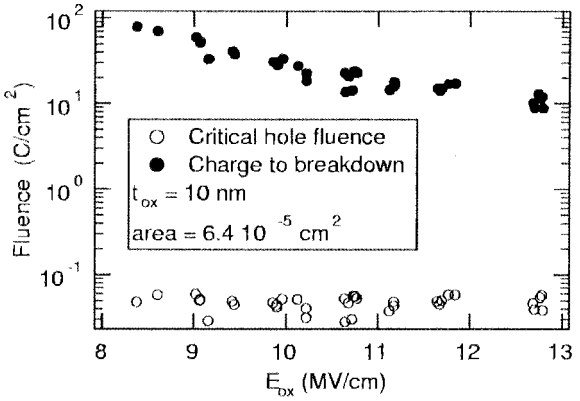


FIG. 53. Charge to breakdown, Q_{BD}, and the hole fluence at breakdown, as a function of electric field. The hole fluence at breakdown is constant in the measured field range, although Q_{BD} decreases continuously in the same range [from Degraeve *et al.* (Ref. 3)].

recently experimental evidence supporting this model has been presented.[359] The hole current density can be related to the electron current density, J_n, as follows

$$J_p = \alpha(E_{ox}) J_n , \tag{4}$$

where $\alpha(E_{ox})$ is the field dependent hole generation efficiency. In the anode hole injection model, α is interpreted as the probability for a tunneling electron to generate an anode hole which is injected back into the oxide towards the cathode.[356] Under constant voltage stress, α is found to be almost constant,[330] while under constant current stress, α increases slightly. However, for thin oxides the difference between the initial and final values of α is very small. Therefore an approximate equivalent relation to Eq. (4) also holds for the integrated values of J_p and J_n, the hole fluence, Q_p, and the electron fluence, Q_n:

$$Q_p = \alpha(E_{ox}) Q_n . \tag{5}$$

Chen *et al.*[354] observed for the first time that the hole fluence reaches a critical value at breakdown, designated $Q_{p,crit}$. This result has been confirmed,[360,361] and further, substrate hot hole injection experiments indicate that a critical hole fluence is needed to trigger oxide breakdown.[362,363] In Fig. 53, $Q_{p,crit}$ and Q_{BD}, measured over a wide field range of 8–14 MV/cm, are plotted. Clearly, $Q_{p,crit}$ remains constant over the entire field interval, while Q_{BD} decreases with increasing field. A satisfactory physical explanation for the experimentally observed invariance of $Q_{p,crit}$ cannot be found in the literature, but the various suggested possibilities will be discussed in detail in Sec. III B 6.

It should be noted that in the work of Satake *et al.*,[360] $Q_{p,crit}$ was observed to be constant only at 300 K; at lower temperatures it decreased as a function of the field. This observation is consistent with the findings of Kaczer *et al.*,[364] where an increase as a function of field is found for temperatures above 300 K. These temperature effects indicate that the hole fluence at breakdown is possibly not the determining factor for breakdown.

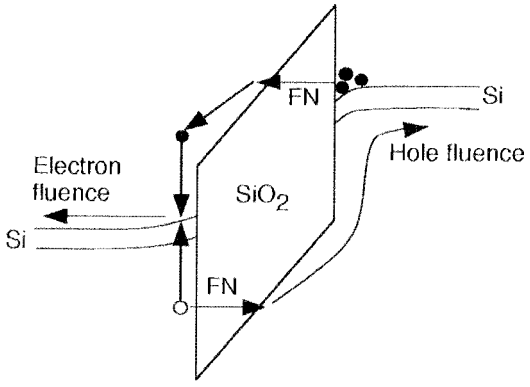


FIG. 52. Schematic illustration of the anode hole injection model. Injected electrons reach the anode with high energy and can generate hot holes that can tunnel back to the cathode, giving rise to the substrate current. FN refers to Fowler–Nordheim tunneling [from Degraeve *et al.* (Ref. 3)].

4. Neutral electron trap generation

During oxide stressing, neutral electron traps are generated in the oxide.[365,366] Although many researchers have related such trap creation to the breakdown process, direct measurements of the oxide neutral trap density, D_{ot}, as a function of the applied stress conditions, are not commonly done. In order to measure this degradation phenomenon, the neutral traps have to be made electrically visible. This can be accomplished by periodically interrupting the stress to fill the generated traps with electrons, without creating any additional traps. A technique ideally suited for this purpose is uniform substrate hot electron (SHE) injection.[367–369] In some cases[368,369] the necessity of a trap filling step is demonstrated. Indeed, immediately after stress, a majority of the available oxide traps are neutral, and further, the probability of occupancy depends on the applied stress field. Therefore the trapped charge, measured immediately after stress, is not a good indication of the neutral trap density.

Substrate hot electron injection can also be used to stress the oxide in a field range below the practically accessible FN field range.[345,370] In Fig. 54, the neutral trap density increase is shown as a function of the injected fluence. Degradation and breakdown in the field ranges of 6.0–8.5 MV/cm with SHE injection and 8.5–11.0 MV/cm with constant voltage FN injection are presented. The fraction of filled traps after SHE injection is found to be constant for all stress fields.[345]

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

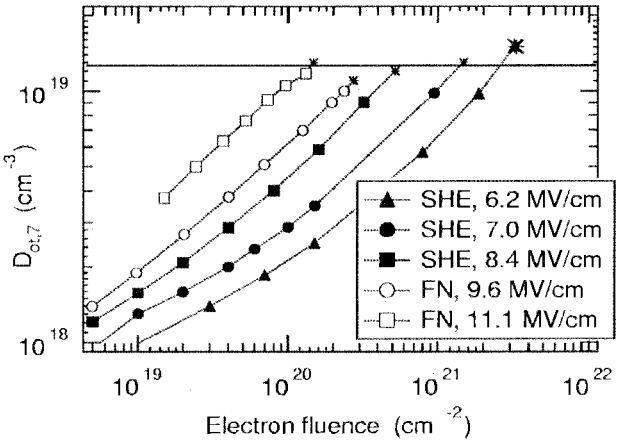


FIG. 54. Occupied electron traps at a filling field of 7 MV/cm, $D_{ot,7}$, as a function of the injected electron fluence measured during oxide stressing at fields between 6.2 and 11.1 MV/cm. Oxide stressing was performed either by Fowler–Nordheim (open symbols) or substrate hot electron injection (closed symbols). For each stress condition, the mean breakdown value is indicated by an asterisk [from Degraeve *et al.* (Ref. 345)].

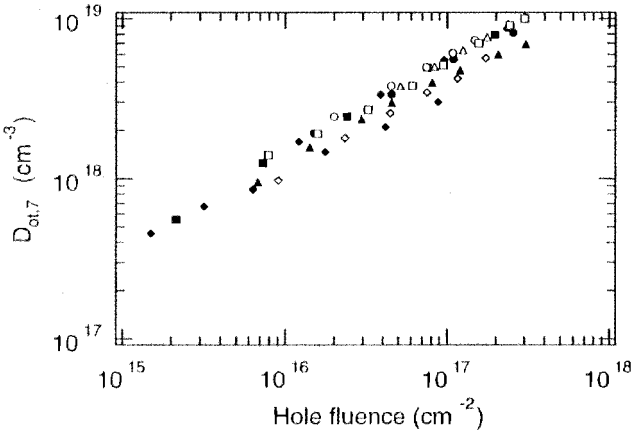


FIG. 55. Generated neutral electron traps, $D_{ot,7}$, as a function of the hole fluence for different oxide thicknesses (7–14 nm), stress types (constant voltage and constant current), and oxide fields (9.5–12 MV/cm). A unique relationship is observed [from Degraeve *et al.* (Ref. 345)].

In the field range under consideration, breakdown occurs when D_{ot} reaches a critical value, within some small statistical fluctuation. This result supports the idea that a critical electron trap density is necessary to trigger breakdown.

A breakdown model based on neutral trap generation has been proposed by several authors.[55,345,365,371–373] It is assumed that at some place on the capacitor the local trap density becomes sufficiently large to allow the formation of a conductive chain of traps connecting the anode with the cathode interface. This model will be investigated in further detail in Sec. III C 1.

In Fig. 55 the generated neutral trap density has been plotted as a function of hole fluence for different oxide thicknesses and FN stress conditions. A unique relationship is observed, independent of oxide field and thickness.[345] Thus it can be concluded that the critical hole fluence, $Q_{p,\mathrm{crit}}$, corresponds to a critical generated density of neutral electron traps, $D_{\mathrm{ot,crit}}$, proving that both breakdown criteria are equivalent.

5. Stress-induced leakage current

The fifth phenomenon that occurs during oxide degradation is the generation of a SILC through the gate. Stress induced leakage current is illustrated in Fig. 56, where I_g-V_g curves from fresh and stressed samples are shown. The SILC rises continuously with injected fluence, and its V_g dependence can be empirically fitted with a FN expression using a barrier height of 1 eV.[374–377] When the SILC is continuously monitored as a function of time after a given stress, two components can be distinguished.[366,378] Initially, a decaying transient component is observed, leading to a steady state SILC after some time. Both components depend on oxide thickness, as is illustrated in Fig. 57. Thick oxides have a large transient component and low steady state component, whereas ultrathin oxides have a very small transient component and a large steady state component.

The SILC itself is in some cases an important reliability problem. Leakage current through the gate translates to a power waste problem in MOSFETs, resulting, for example, in having to constantly charge the batteries of portable devices. Such leakage is especially detrimental to the performance of nonvolatile memories. When the charge stored on the floating gate leaks off, the threshold voltage of the cell shifts and the stored information is lost after some time.[366,375,379,380]

The transient component of the SILC results from emptying negatively charged traps immediately after stress. A simple tunneling model predicts a $1/t$ decay of this current.[365] In recent publications, however, it has been shown that, apart from the electron component, a hole component is also present in the transient current. Consequently, the electron transient current was found to follow a $1/t^n$ dependence with $n<1$.[381] Substrate hot electron[381] and channel hot electron injection[382] experiments further confirm the role of the hole component in the transient SILC. The steady state component of the SILC is caused by trap-assisted tunneling from cathode to anode. In thick oxides the probability that an electron can use traps as ''stepping stones'' for tunneling is very small, resulting in a small steady state SILC component. In thinner oxides, fewer traps are necessary for the electrons to move from cathode to anode, and therefore the steady state

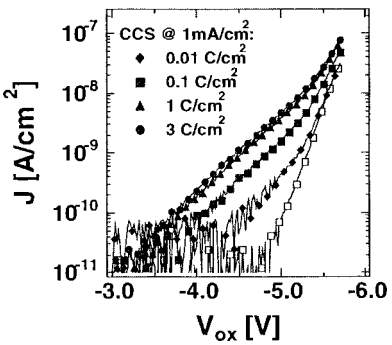


FIG. 56. Gate current density as a function of applied voltage for an unstressed device (open symbols) and after various high field stresses have been applied (solid symbols). A gradually increasing leakage current, called the stress induced leakage current, appears at low voltage [from Degraeve *et al.* (Ref. 3)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

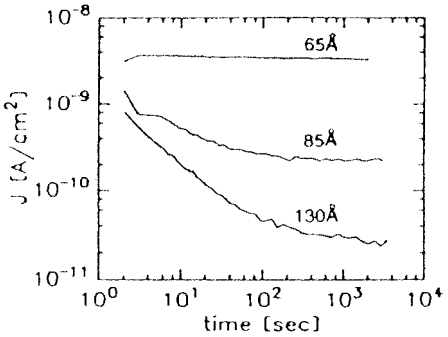


FIG. 57. The oxide thickness dependence of the steady state and transient components of stress induced leakage current. As the oxide thickness increases, SILC is transformed from a steady state to a transient current. The current is measured at a field of 5.4 MV/cm following a stress at 9.5 MV/cm for 20–30 C/cm^2 [from Moazzami *et al.* (Ref. 378)].

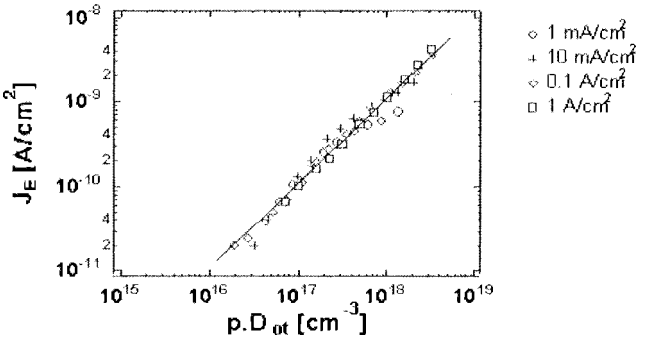


FIG. 59. The steady state stress induced leakage current measured at a fixed field of 5 MV/cm, plotted as a function of the generated density of neutral traps. Independent of the stress condition, a one-to-one relation is observed [from DeBlauwe *et al.* (Ref. 379)].

component will dominate.[383] Modeling of the SILC trap-assisted tunneling process has been the topic of recent publications.[384,385]

In ultrathin oxides, a new SILC component, arising from electrons that tunnel directly into interface traps, is observed.[343,386] This leakage current is relatively large in the low voltage range, close to the flatband voltage, as illustrated in Fig. 58. In Fig. 59 the close relationship between SILC and the oxide trap density is illustrated. To gather this data, the FN stress was periodically interrupted to measure the leakage current density J_E at a fixed low oxide field E, while on the same device the density of neutral oxide traps was determined.[345] Plotted against each other, a stress-independent, one-to-one relationship is revealed between the steady state SILC increase and the generation of neutral traps.[379] Several other authors have emphasized the relation between the neutral trap density and the SILC,[57,376,387] but very recently this relationship has been questioned.[388] Despite these recent observations, many authors consider SILC to be a measure of the neutral trap density. Consequently, SILC, either bulk trap or interface trap related, has been used as a degradation monitor and time-to-breakdown predictor.[54,60,347,389–391]

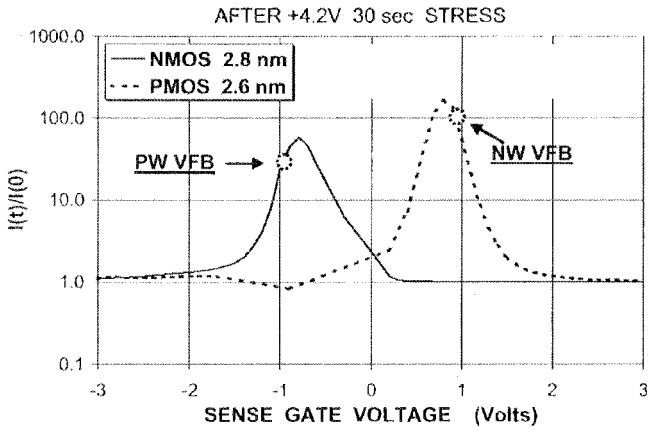


FIG. 58. Poststress $I-V$ curves comparing N and P metal–oxide–semiconductor devices. In both cases the peak degradation occurs near the flatband voltage. The current increase is primarily observed when the sense voltage is within 1 V of the flatband voltage [from Nicollian *et al.* (Ref. 386)].

6. Discussion of trap generation mechanisms

It is clear from the results shown in the previous sections that trap generation is the key factor determining oxide degradation and breakdown. Here, we compare three trap generation models: the ''anode hole injection model,'' the ''electrochemical model,'' and the ''H release model.''

In the anode hole injection model,[356] illustrated in Fig. 52, it is assumed that holes tunneling back to the cathode can create electron traps in the oxide, probably in conjunction with an electron in the SiO_2 conduction band. The physics of the trap creation process is still speculative. There have been several studies demonstrating that the interaction of electrons and holes in an oxide results in trap creation.[360,392–394] However, the precise role of electrons and holes in the trap creation process and the details of the microscopic mechanism are still uncertain. The most important difficulty in studying this effect is the inability of most techniques to separately control the hole and the electron injection.

Electrons injected in the oxide may lower their energy by light emission.[395,396] Experimental evidence has been presented that photoexcitation of valence band electrons in the cathode by light generated in the anode, and not anode hole injection, is the dominant source of the measured holes in the substrate.[358,359,396] If this is correct, or if there exists a voltage limit to anode hole injection,[358] it could be questioned whether the anode hole injection model will correctly predict low voltage oxide reliability. Recent modified simulations[397,398] of anode hole injection show the existence of an exponentially decaying impact ionization rate at low voltage, which corresponds to the exponentially decaying trap generation rate measured by SILC.[54]

According to the anode hole injection model, the observation of a unique relation between hole fluence and neutral electron trap generation (Fig. 55) is interpreted as a causal relation, i.e., the holes are necessary to create the traps. This mechanism is outlined in Fig. 60(a). However, other explanations are possible. As is outlined in Fig. 60(b), energy release of the incoming electrons at the anode can, beside hole creation, also activate some other mechanism that is

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

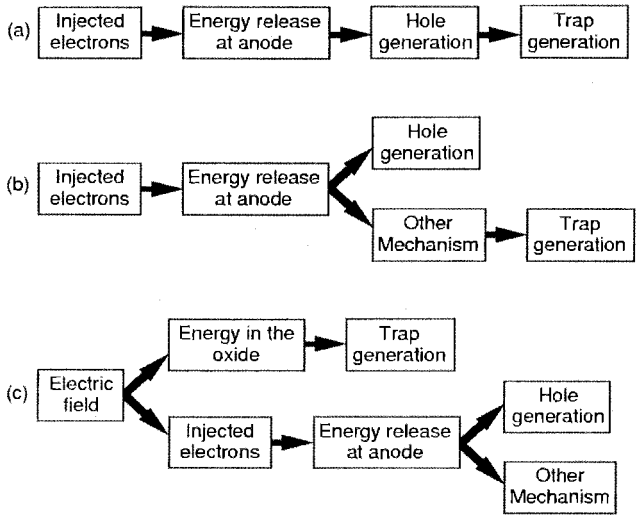


FIG. 60. Outline of three neutral electron trap generation mechanisms currently discussed in the literature.

responsible for neutral electron trap generation. This suggests that the hole fluence and the trap creation have a common origin, i.e., the energy released by the electrons at the anode, but not a causal relationship.

A second model, named the ''electrochemical'' model,[365,399–403] is illustrated in Fig. 60(c). Here, the electric field itself directly induces electron trap creation in the oxide. According to this interpretation, all processes that are related to the energy release of the injected electrons at the anode are independent of the trap generation mechanism. Furthermore, the electron fluence has no impact on the trap generation rate. A trap creation mechanism based on the interaction of oxide dipoles with the electric field has been proposed.[401,402]

A third model for the mechanism depicted in Fig. 60(b) is H release at the anode. Most older publications[341,404] on this issue deal with interface trap creation at the cathode, but the model's basic ideas can easily be extended to bulk oxide traps. In the H release model, the electrons tunnel through the oxide potential barrier and reach the anode with sufficient energy to release H from the anode/oxide interface. Hydrogen is always present in sufficient amounts due to forming gas (N_2/H_2) anneals, a standard practice to reduce the initial interface trap density. The released H diffuses through the oxide and can generate electron traps. Again, as for the anode hole injection model, the precise physical details of the microscopic trap generation mechanism with H are subject to speculation. An interesting argument in favor of the H release model is provided by the work of Cartier *et al.*[405] An oxide, without a polycrystalline Si gate, is exposed to a remote H plasma. It is observed that trap creation at the Si/SiO_2 interface evolves identically to the interface trap creation induced by a hot electron stress. On the other hand, some recent experiments using D-annealed samples provide no support for the H release model,[406] although a clear isotope effect, measured by SILC and flatband voltage changes, has been observed.[407,408]

C. Oxide breakdown

Thus far we have discussed oxide degradation phenomena during electrical stress. In this section we focus on the breakdown event itself. First, the modeling of the breakdown event will be discussed. Then, the occurrence of so-called soft breakdown in ultrathin oxides, and its relationship to device failure, will be addressed.

1. Breakdown modeling

As early as 1990 a ''weakest link'' breakdown model had been proposed.[373,409,410] In this model, a capacitor is divided into a large number of small cells. It is assumed that during oxide stressing neutral electron traps are generated randomly over the capacitor area. The number of traps in each cell is counted, and at the moment the number of traps in one cell reaches a critical value, breakdown occurs, by definition. In other words, in that critical cell the number of traps is sufficiently large to create a conductive path from anode to cathode.

A disadvantage of this model[373] is its two-dimensional nature. Therefore a new ''weakest link'' model based on percolation theory principles[411] has been proposed that can accurately describe the intrinsic breakdown distribution. The use of the percolation concept for oxide breakdown modeling has been suggested[412] and thoroughly elaborated upon.[53,55,344,345] The percolation model for breakdown exists in two versions: (i) the sphere model, where each generated defect in the oxide is characterized by a sphere with radius 0.9 nm, and (ii) the cube model, where each defect is represented by a cube whose edge is 1.3 nm in a three-dimensional frame. Both models are implementations of the same concept and provide, therefore, similar results. As an example, the sphere model[344] is schematically illustrated in Fig. 61. It is assumed that electron traps are generated inside the oxide at random positions in space. Around these traps a sphere is defined with a fixed radius r, the only parameter of the model, Fig. 61(a). If the spheres of two neighboring traps overlap, conduction between these traps becomes possible. Further, the two interfaces are modeled as an infinite set of traps, Fig. 61(b). This mechanism of trap generation and coalescence continues until a conducting path is created from one interface to the other, which is the definition of breakdown in this model, Fig. 61(c). In a computer simulation, the total electron trap density needed to trigger breakdown, $D_{\mathrm{ot,crit}}$, can now be calculated. It is found that the simulated $D_{\mathrm{ot,crit}}$ distribution can be fitted with a Weibull function.[53]

The percolation model of breakdown is able to quantitatively explain two important experimental observations: (i) as the oxide thickness decreases, the density of oxide traps needed to trigger breakdown decreases,[56,345,369] and (ii) as the oxide thickness decreases, the Weibull slope, β, of the breakdown distribution decreases, i.e., a larger spread of the t_{BD} values is observed.[55,344,345,413] The latter effect is illustrated in Fig. 62. An important consequence of the decreasing Weibull slope for thinner oxides is the strongly enhanced area dependence of t_{BD} or Q_{BD}.[345,413] Indeed, based on the random nature of the breakdown location, it has been shown that for the scale factors η_1 and η_2 of two Weibull distribu-

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

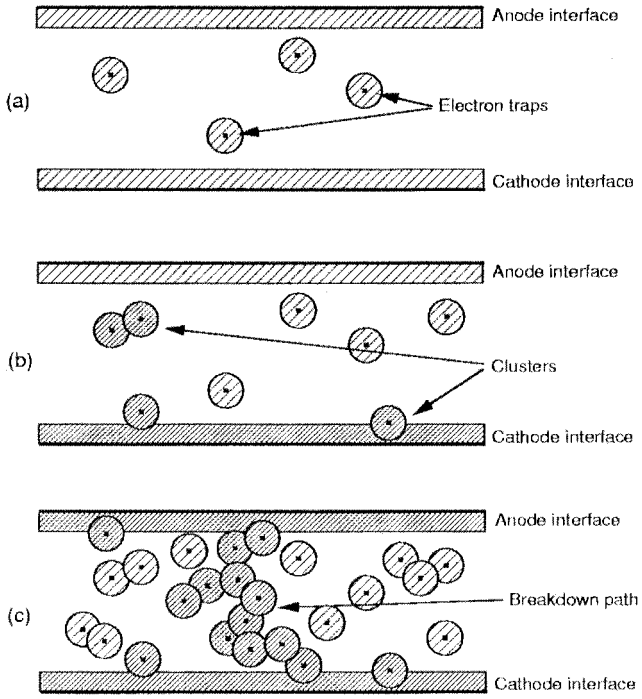


FIG. 61. Various steps of the percolation model for oxide breakdown. As the density of neutral electron traps increases, conductive clusters of traps are formed, ultimately leading to the creation of a conductive breakdown path from anode to cathode [from Degraeve *et al.* (Ref. 3)].

tions (either t_{BD} or Q_{BD} distributions) of capacitors with identical oxide thickness, but area A_1 and A_2, respectively, the following relationship holds:[414,415]

$$\frac{\eta_1}{\eta_2}=\left(\frac{A_2}{A_1}\right)^{(1/\beta)}. \tag{6}$$

Equation (6) predicts that as β decreases, the area dependence of Q_{BD} will be enhanced. This is illustrated in Fig. 63 for films of varying thickness. It can be concluded that for thick oxides ($t_{ox}>10$ nm), the intrinsic Q_{BD} value is, within acceptable approximation, constant in the range of capacitor areas commonly available for experimental purposes. However, for thin oxides Q_{BD} can no longer be considered area independent. This has important implications when the Q_{BD}

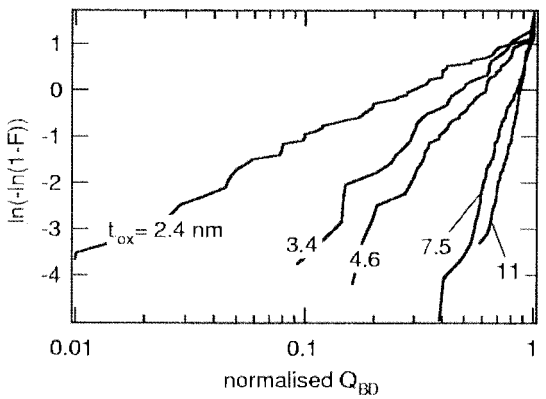


FIG. 62. Normalized Q_{BD} (charge-to-breakdown) Weibull distributions for oxides of different thickness. The decrease of the slope with decreasing oxide thickness is clearly observed [from Degraeve *et al.* (Ref. 345)].

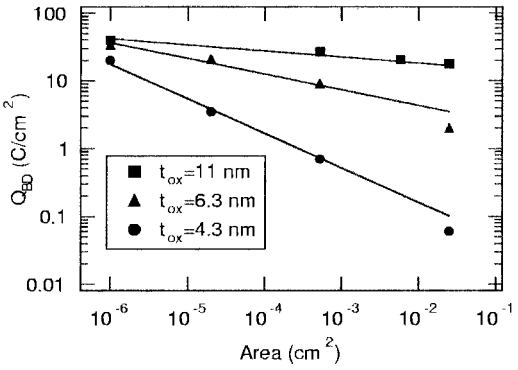


FIG. 63. The 63% value of Q_{BD} (charge-to-breakdown) as a function of the area of the test capacitor, for different oxide thicknesses, under gate injection. As the oxide thickness decreases, a stronger area dependence is observed [from Degraeve *et al.* (Ref. 345)].

value is used as the figure of merit for the oxidation process, a common industrial practice. It is meaningless to specify a Q_{BD} value without specifying the area, and it is further necessary to specify the area when Q_{BD} values of different oxide thicknesses are compared.

2. Soft breakdown

Breakdown in oxides of thickness greater than 5 nm proceeds by the creation of a localized conductive path, followed immediately by the propagation of thermal damage leading to a highly conductive short between anode and cathode. On the other hand, it has been known for several years that ultrathin oxides can exhibit anomalous failure,[374] characterized by the creation of a more resistive breakdown path. This phenomenon has been termed soft, quasi, early, or nondestructive breakdown, or B-mode SILC. Only recently has this breakdown mode gained much attention in sub-4 nm oxide layers.[61,416–428] Soft breakdown (SBD) can be defined as oxide breakdown without lateral propagation of the breakdown spot due to thermal damage.[418] It is generally accepted that soft and hard breakdown originate from the same precursor defects,[3,425,429] show the same stress current dependence,[427] and can be described by the same Weibull statistics,[429,430] although the latter point has recently been called into question.[431]

It has been shown that the I_g after soft breakdown has a unique relationship with V_g, i.e., it is independent of area, suggesting that soft breakdown is a localized effect.[421] Figure 64 shows a typical example of an I_g-V_g plot, after soft breakdown. A dramatic rise compared to SILC is observed, but the SBD is less destructive as compared to hard breakdown. This conclusion has been confirmed by emission microscopy experiments.[422] However, for very small area devices, a lower, unstable current is measured.[421] This might be explained by the difference in energy available for discharge at the moment of breakdown. Typically, when the applied voltage is plotted as a function of time during CCS, a very small drop in the voltage (or equivalently a small jump of the current during CVS), followed by noisy behavior, signals soft breakdown. However, the small voltage jump observed during FN stress is not a characteristic feature of soft breakdown, although often claimed as such in the literature. In

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

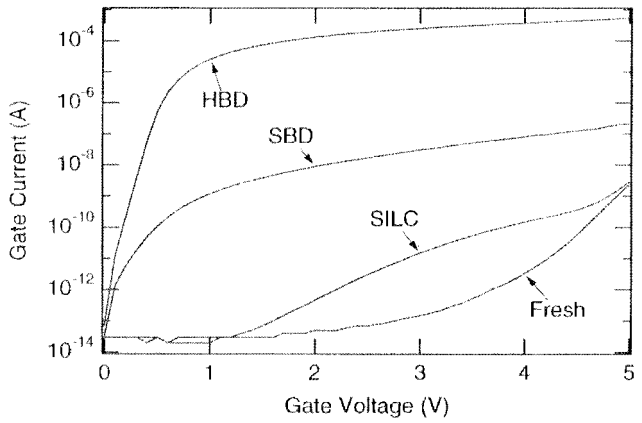


FIG. 64. I_G-V_G curves for a capacitor with an oxide thickness of 4.5 nm. A comparison is made between the current in the fresh device, after stressing (stress induced leakage current, SILC), and after soft (SBD) and hard (HBD) breakdown [from Crupi *et al.* (Ref. 421)].

fact, when the test structure area is scaled down, the voltage jump is of the order of volts.[421] On typical large area test structures, the small voltage or current jumps indicating soft breakdown become very difficult to detect with automated measurement systems. Therefore other breakdown detection methods have been proposed. The most effective one is the use of the sudden increase of the gate current noise as the detection monitor.[61] This noise has been studied extensively.[421,423,424,427,432,433] At low gate voltage, multilevel random telegraph signals are observed with current amplitudes that depend on the applied gate voltage, shown, for example, in Fig. 65. It has been demonstrated that the $I-V$ characteristics of the on and off states are shifted over a constant voltage interval.[421] This observation can be explained by electron capture-emission-induced local field fluctuations in the breakdown path.[421,423] With this model, the area of the soft breakdown site is estimated to be $2\times10^{-13}\,\mathrm{cm}^2$.[421]

The current conduction mechanism through the soft-broken region in the oxide has been modeled in several ways, but the physical picture remains unclear. Models based on variable range hopping of carriers,[390,419] point contact conduction,[434,435] energy funnels,[420] resonant tunneling through strategically placed traps,[436,437] direct tunneling through a thinned oxide region,[417,438] and electrode controlled conduction[433] have been proposed.

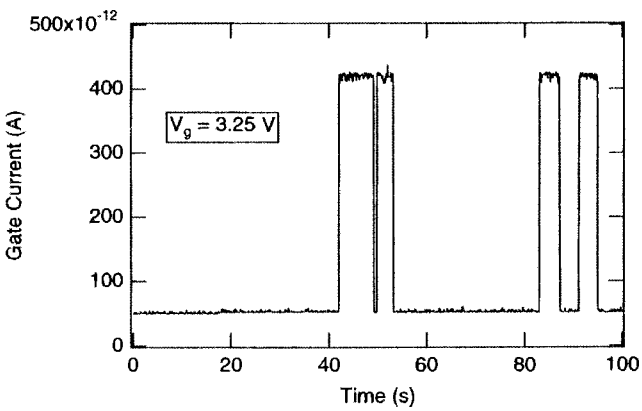


FIG. 65. An example of a two level random telegraph signal in the gate current of a capacitor after soft breakdown [from Crupi *et al.* (Ref. 421)].

Some researchers have claimed that soft breakdown does not occur in short channel length transistors; instead, hard breakdown is immediately observed.[425] However, soft breakdown has been demonstrated in 50 nm gate length devices[439] and has been shown to depend on applied voltage, not gate length.[428] It has been further claimed that after soft breakdown no significant variations in MOSFET I_d-V_g characteristics can be observed and therefore, for some applications, soft breakdown does not necessarily imply device failure.[61,439] In determining the relationship between soft breakdown and device failure, the position of the breakdown spot is extremely important. Breakdowns which occur in the drain/gate overlap region have been shown to more profoundly affect transistor function than breakdowns in the middle of the transistor.[426,440] However, the most recent evidence points to devices being operational after soft breakdown if operated at low voltage and current, such as would be the case in an actual circuit.[441,442]

3. Breakdown acceleration models

The most important issue for the analysis of t_{BD} data, in order to predict oxide reliability, is the choice of the proper, i.e., field or voltage, extrapolation law. Indeed, oxide reliability has been pinpointed as one of the possible showstoppers in scaling the oxide thickness;[3,54,429,443] however, this prediction was based on t_{BD} values measured at very high fields, whereas actual devices operate at much lower voltages and fields. The correctness of the oxide reliability prediction at actual operating conditions depends completely on the validity of the extrapolation law.

There have been contradictory opinions on the exact field dependence for t_{BD}. Some research groups claim that based on the anode injection model, the logarithm of t_{BD} scales with $1/E_{\mathrm{ox}}$, whereas others find better results using an E_{ox} dependence. Most recently, a V_g dependence has been proposed for ultrathin oxides where ballistic transport of electrons through the oxide occurs. According to the anode hole injection model,[354–356] the field dependence of α, the probability of creating a hole which can tunnel back into the oxide (see Sec. III B 3), can be described as

$$\alpha=\alpha_0\exp\left(\frac{-H}{E_{\mathrm{ox}}}\right)$$

and

$$Q_{\mathrm{BD}}=Q_0\exp\left(\frac{H}{E_{\mathrm{ox}}}\right) \tag{7}$$

with α_0 and H constants (for a fixed oxide thickness) and $Q_0=Q_{p,\mathrm{crit}}/\alpha_0$. With this equation, t_{BD} becomes

$$t_{\mathrm{BD}}=\frac{Q_{\mathrm{BD}}}{J_{\mathrm{FN}}}\approx\frac{Q_{\mathrm{BD}}}{A^*}\exp\left(\frac{B^*}{E_{\mathrm{ox}}}\right)=\frac{Q_0}{A^*}\exp\left(\frac{B^*+H}{E_{\mathrm{ox}}}\right)$$
$$=\tau_0\exp\left(\frac{G}{E_{\mathrm{ox}}}\right) \tag{8}$$

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

with τ_0 a constant. Reported values for $G=B^*+H$ vary from 290 to 350 MV/cm, depending on oxide thickness and stress type (constant voltage or current stress). Equation (8) expresses the $1/E$ model, because the logarithm of t_{BD} depends linearly on the reciprocal oxide field. The E model, on the other hand, predicts a linear relationship between the logarithm of t_{BD} and the oxide field:[400,402,403]

$$t_{BD}=t_0 \exp(-\gamma \cdot E_{ox}), \tag{9}$$

where t_0 and γ are constants. The E model had been used long before there existed any physical data to support it. In the literature, publications trying to prove the correctness of either the E or the $1/E$ model can be found,[361,403,410,444–446] as is illustrated in Fig. 66.

All attempts to provide the E model with a sound physical basis assume that a direct correlation exists between the electric field and oxide degradation. Therefore proponents of this model ignore the role of injected electrons as an intermediate step for generating oxide traps [see Sec. III B 6, Fig. 60(c)]. Recent experiments clearly demonstrate that the oxide degradation process is fluence driven.[447,448] Furthermore, detailed simulations of anode hole injection, including minority carrier ionization,[397,398] no longer link a $1/E$ model directly with the anode hole injection concept. Instead, a mixed model, with approximate $1/E$ dependence at high voltage and E dependence at low voltage, is used. Other groups have proposed similar unified models.[449–452]

The E vs $1/E$ model discussion is mainly valid for oxides thicker than 5 nm, where the injection of electrons is dominated by nonballistic FN injection; the injected electrons enter the conduction band of the SiO_2 and interact with it. The oxide field mainly determines the electron energy at the anode and consequently, the oxide degradation. Since there exists a unique relationship between the FN current density and oxide field, Q_{BD} should be measured using CCS. For ultrathin oxides, however, the injected electrons travel ballistically through the oxide without interacting with the SiO_2 network. This can be either by FN tunneling above 3.5 V, typically in oxides with thicknesses of between 5 and 3.5 nm, or by direct tunneling below 3.5 V, typically in oxides with thicknesses of below 3.5 nm. The electron energy at the anode is determined by the voltage difference between the cathode and the anode, which corresponds to the applied gate voltage.[398,447,453] As a consequence, Q_{BD} should be measured using CVS.[453] This also means that for an ultrathin oxide the gate voltage determines the breakdown, and CCS methodology needs to be replaced by CVS analysis.[347,453]

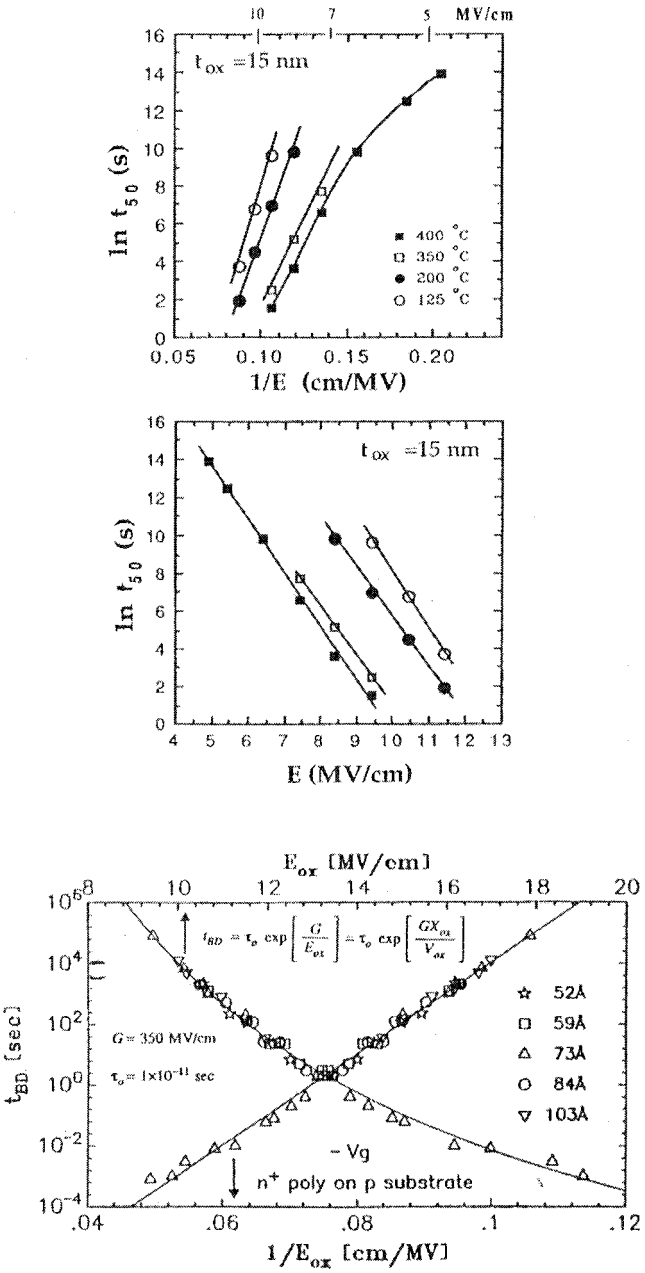


FIG. 66. Two data sets from the literature, one supporting the E (field) extrapolation model [two top figures, from Suehle *et al.* (Ref. 444)] and the $1/E$ model [lower figure, from Schuegraf *et al.* (Ref. 445)].

4. Temperature dependence of breakdown

Since advanced CMOS integrated circuits operate somewhat above ambient, the temperature dependence of oxide degradation and breakdown has received considerable attention. The temperature dependence of t_{BD} in ultrathin oxides is especially strong,[364] as is illustrated in Fig. 67. In most research, it is assumed that an Arrhenius law can describe the temperature dependence of t_{BD}, and many authors have determined the activation energy for their oxides. The activation energies depend, however, on the oxide thickness,[454] the voltage or field range,[446] and the temperature range[350,455,456] of the measurement. From the huge spread of the observed values it can be concluded that the Arrhenius relationship is not suitable as a description for the temperature dependence of t_{BD}.[364,457,458] However, both the trap density at breakdown as well as the trap generation rate depend on temperature,[458] although the oxide traps created at different temperatures are not completely equivalent and consequently, oxide damage generated during electrical stress at different temperatures is not simply cumulative.[364]

5. Oxide reliability predictions

Accurate predictions of oxide reliability can only be obtained if a correct and complete reliability specification is defined. This specification must contain four elements: the

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

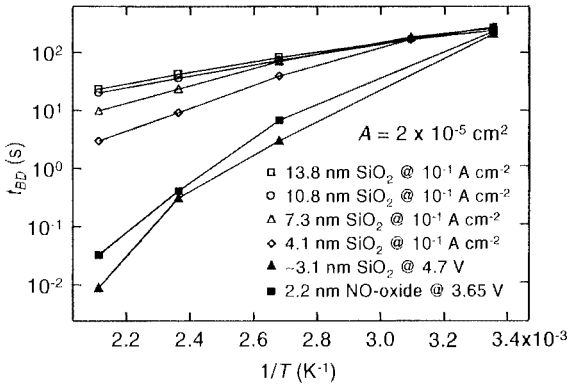


FIG. 67. Arrhenius plots of time-to-breakdown for oxides of various thicknesses. The results reveal that no single activation energy can be determined and that the thinner the oxide the higher the activation energy [from Kaczer *et al.* (Ref. 364)].

allowed failure rate, expected lifetime, the oxide area, and the voltage and temperature conditions. A typical specification reads: 0.01% failures are allowed after 10 years of dc operation, at 1.5 V and 70 °C, on a device of area 0.1 cm^2. With similar specifications, it has been reported that a reliability limit for oxide thickness scaling is encountered at about 2.2 nm (optical thickness) at room temperature.[54,443] Recent work has shown these predictions to be overly pessimistic. Improved accuracy of the voltage acceleration law, as well as oxide uniformity improvements, have shifted the reliability limit to oxides as thin as 1.5 nm.[62,459]

IV. FABRICATION TECHNIQUES FOR ULTRATHIN SILICON OXIDE AND OXYNITRIDES

The gate dielectric's ultimate electrical performance is determined not only by its composition (SiO_2 vs Si–O–N) and fabrication method (growth, deposition, or implantation), but also by pregrowth surface preparation and postfabrication processing such as plasma etching of the gate stack. The interdependence between the various steps, especially surface preparation, becomes more prominent for ultrathin gate dielectric layers, since the Si/SiO_2 interface is a more significant part of the layer as it gets thinner.

A. Surface preparation

Surface preparation is a more appropriate term than cleaning, since preparation of the Si surface for subsequent oxidation is far more involved than merely removing contamination.[460] In fact, engineering of the surface, i.e., conditioning it to result in its smoothest, cleanest, and most unperturbed state, is just as important a step as the actual dielectric fabrication. Silicon surface preparation has been the subject of exhaustive work.[461–468] Among the important physical attributes of ultrathin SiO_2 layers and the Si/SiO_2 interface that can be influenced by surface preparation are interfacial roughness,[469–471] interfacial transition layer width,[180] contamination level of the SiO_2 and the interface,[472–474] and chemical bonding structure at the interface.[104,124,475] Figure 68 is an example of the effect of various cleans on the surface roughness and reliability of ultrathin oxides.

Wet cleaning currently dominates pregate oxidation clean applications.[476] The so-called "RCA" chemistry is the most widely used clean for removing organic compounds and metals from Si wafers.[461,464] Subsequent processing in HF, which removes the chemical oxide that results from the RCA clean, is optional. Although much research has gone into understanding wet cleaning chemistry, there is still much to learn about the effects of the various chemistries on the electrical properties of the resultant dielectrics. This is a fertile area for continued research.

Dry cleaning technology, so called because it involves vapor or gas, and not liquid cleaning of the wafer surfaces, is presently the subject of much research.[477–479] This is driven in part by the much lower consumption of chemicals in dry versus wet processing (and the need to dispose of them in an environmentally sensible manner), but primarily by the drive towards *in situ*, cluster tool processing. A typical gate cluster tool, with pregate dielectric clean, and dielectric and polycrystalline Si growth modules, is shown in Fig. 69. Some research has already demonstrated oxide reliability increases due to dry pregate oxide cleans.[469,480,481] Further, comparison of Si/SiO_2 roughness, as measured by AFM[469] as well as STM,[482] has shown that *in situ* dry cleaned surfaces may be smoother than wet cleaned samples.

B. Fabrication of ultrathin oxide and oxynitrides

Fabrication of ultrathin dielectric layers may be accomplished by growth, deposition, or implantation. Growth refers to thermal oxidation or oxynitridation of the Si. Deposition usually refers to chemical or physical generation of the layer, not involving a reaction with the Si substrate. Some processes are combinations of deposition and growth, e.g., low energy implantation of Si with N, followed by thermal oxidation in O_2. Table VI is a compilation of published fabrication techniques for SiO_2 and Si–O–N gate dielectrics.

1. Thermal oxidation and oxynitridation

The utter simplicity of growing thermal SiO_2 by exposing Si to O_2 at elevated temperatures, as well as the perfection of the resulting interface, are in large part responsible for the success of Si as the integrated circuit material of choice. Of course, the quality of the SiO_2 and the Si/SiO_2 interface is in the growth details. Virtually all commercial SiO_2 gate dielectrics are grown by thermal oxidation, using O_2 or H_2O as the oxidant species. Since oxidation in H_2O enhances oxidation kinetics,[483] it is not generally used for the growth of ultrathin films. However, some argue that H_2O-oxidized SiO_2 results in dielectrics with lower defect densities and perhaps enhanced reliability.[484,485] Thermal oxides consume Si during growth, thereby continuously creating a new and fresh interface. Thermal growth usually takes place at a higher temperature than chemical or physical deposition, and higher fabrication temperature has been associated with improved dielectric properties.[486–489] Chemically and physically deposited gate dielectrics usually require postdeposition annealing at temperatures higher than the deposition temperature to attain properties similar to thermal

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

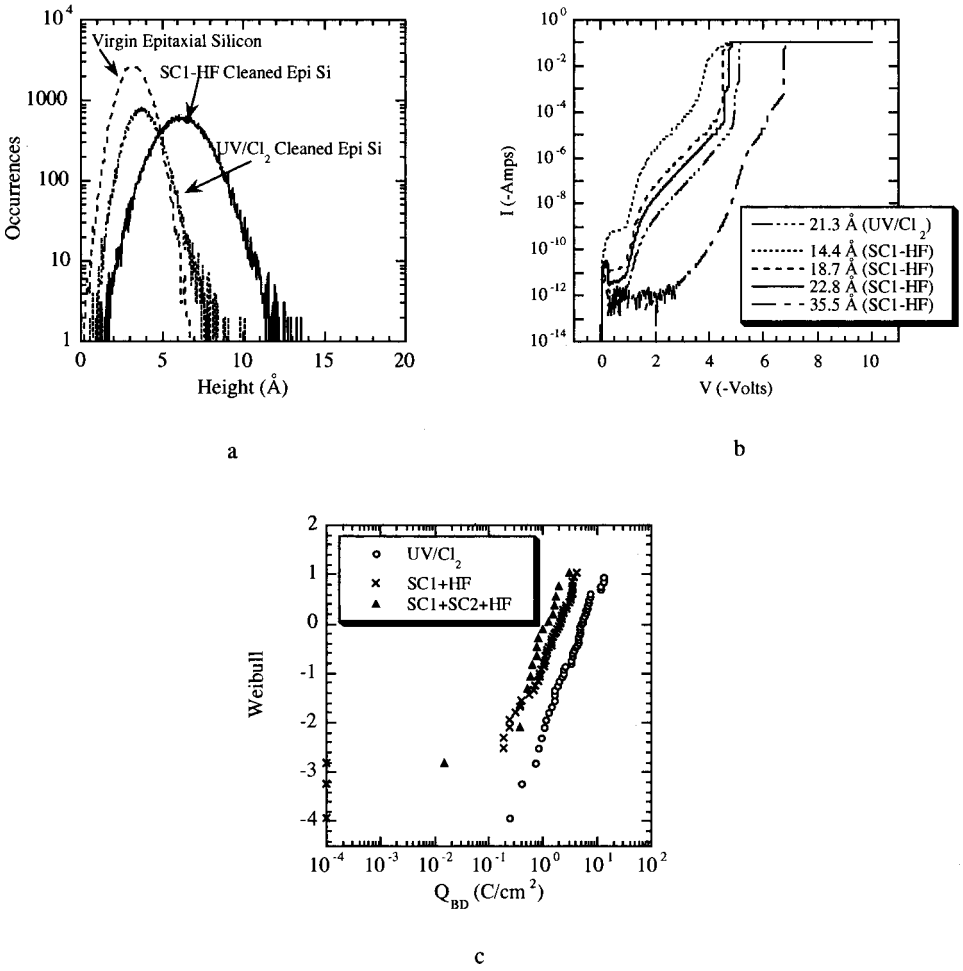


FIG. 68. Effects of various pregate oxidation cleaning schemes on (a) interfacial roughness, (b) leakage current, and (c) reliability of ultrathin SiO_2 gate dielectrics. Note that in this work, dry cleaning (UV/Cl_2) resulted in the best properties. SC1 and SC2 are the two components of the "RCA" chemical clean (Ref. 464) [from Sapjeta *et al.* (Ref. 469)].

oxides.[490,491] Thus attempts to reduce thermal budget by depositing dielectrics at temperatures lower than thermal growth temperatures may be misguided.

Silicon oxidizes according to a linear-parabolic (Deal–Grove) kinetic law, well-described in the literature.[483,492,493] However, this formalism breaks down in the ultrathin film regime, and the details of the first stages of SiO_2 formation are still not well-understood, in spite of much research.[211,494,495] Oxidation mechanisms will be discussed in detail in Sec. V B.

There are currently two primary thermal techniques for growing SiO_2 or Si–O–N, furnace or rapid thermal oxidation (RTO). Oxidation usually takes place in the temperature range of 750–1100 °C. Typical apparatus for both techniques are shown in Figs. 69 and 70. Although there are many ways to input thermal energy into Si to oxidize it, at present vertical furnace technology is the manufacturing standard for

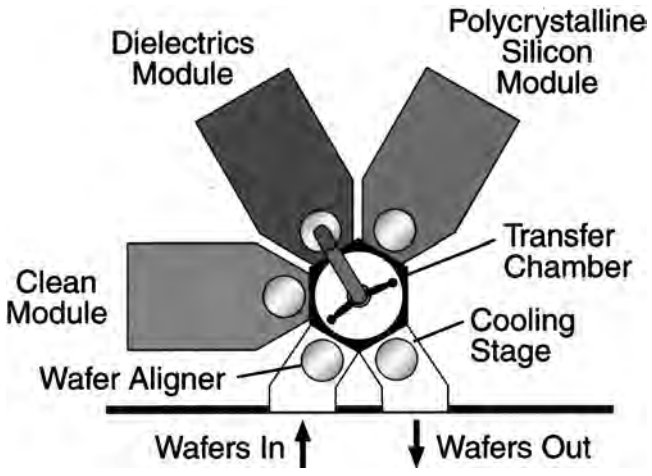


FIG. 69. Schematic of a gate dielectric single-wafer cluster tool showing the loading and unloading ports, and the preclean, dielectric, and polycrystalline Si modules.

TABLE VI. SiO_2 and Si–O–N gate dielectric fabrication techniques.

Thermal oxidation/oxynitridation
O_2, H_2O, O_3
N_2O, NO, NH_3, N_2
Chemical deposition
Chemical vapor deposition (CVD)
Plasma enhanced chemical vapor deposition (PECVD)
Jet vapor deposition (JVD)
Atomic layer deposition (ALD)
Physical deposition
Low energy ion implantation
Remote plasma nitridation

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

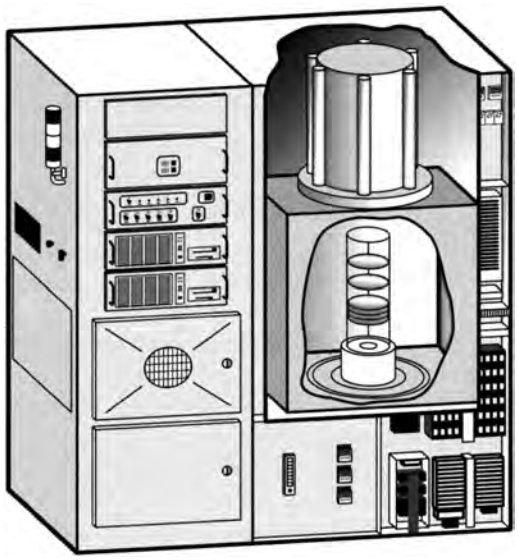


FIG. 70. Schematic of a vertical furnace for the growth of gate dielectrics.

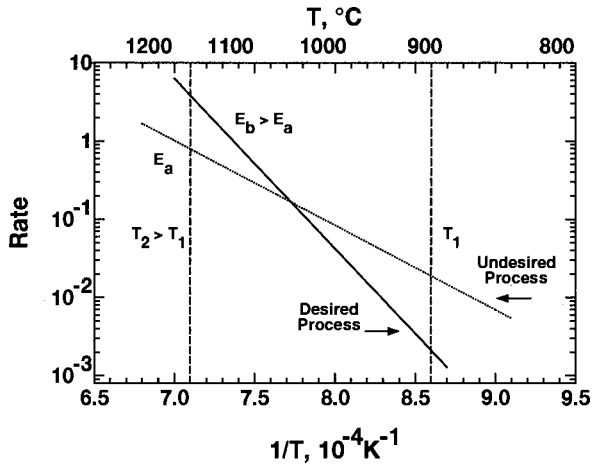


FIG. 71. Arrhenius plot of two competing processes, characterized by different activation energies (E), demonstrating a key advantage of rapid thermal processing: the ability to visit high processing temperatures for short times allows one to favor a desired over an undesired process.

ultrathin oxide growth. (The furnace tube is oriented vertically to improve film uniformity and reduce particulate contamination.) However, the ability to visit a variety of processing temperatures, made possible by the low thermal mass of the single wafer RTO systems, where only the wafer is significantly hot, represents an advantage over furnace technology. The rate of many reaction processes in integrated circuit fabrication, oxidation being typical, is governed by the Arrhenius law:

$$\text{rate} = A \exp(-E_a/kT), \tag{10}$$

where E_a and A are the activation energy and preexponential factor for a given reaction process. When two or more Arrhenius processes can occur at the same time there will be a competition between them, with their relative rates governed by the individual E_a and A terms for each process. A lower E_a yields a faster (relative) reaction at any given temperature, assuming the A terms are similar. For example, it can be seen in Fig. 71 that between two processes having different activation energies, the rate of an undesirable process (e.g., dopant diffusion) can be retarded at higher temperatures with respect to that of a desirable process (e.g., oxidation). Thus a ''desired'' process may be favored in the high temperature regime, not accessible by high thermal mass vertical furnace technology. Fast ramp furnace technology, utilizing small wafer loads, has been developed to fill the gap between single wafer RTO and batch furnace technologies.[496,497]

Vertical furnaces are robust and reliable, offer excellent thickness uniformity, and an isothermal environment in which variations in wafer optical properties, due, for example, to front side lithographic isolation patterns or varying backside layers, play little or no role in wafer temperature uniformity. On the other hand, RTO offers better absolute thickness control for <2.0 nm oxides, a greater processing temperature range, and is ''cluster-friendly,'' i.e., single wafer processing chambers can be integrated for control of interfaces (see Fig. 69). RTO chambers are small and do not attain high temperatures during operation; therefore, integrated processing is readily accomplished. An RTO process, clustered to a pregate oxidation clean, is a likely scheme for growing ultrathin dielectrics in the near future. As dielectrics get thinner, the advantages of *in situ* processing should become apparent, since interfacial effects due to contamination and surface roughness will start to dominate electrical characteristics. Such processing has already succeeded in producing high performance 30 nm (minimum feature size) transistors.[14,482] Figures 72 and 73 are examples of oxidation kinetics attainable in RTO and furnace systems. Thinner oxides, grown at higher temperatures for shorter times, are typical of the RTO process.

Various oxidation gases can be used to grow SiO_2, although the common practice is to use O_2 or H_2O. CO_2 will also oxidize Si to form SiO_2, with some retardation of oxidation kinetics.[498] Ozone (O_3) is sometimes added to the O_2 gas stream to enhance growth kinetics, since atomic O, an ozone decomposition by-product, is very reactive. Low temperature growth ($\leqslant 400\,^{\circ}\text{C}$) is achievable in O_3.[499–503] Oxynitrides, essentially SiO_2 containing small (less than 5%–10% locally, and less than 1% if averaged over the film thickness) but significant amounts of N, can readily be grown using N_2O or NO. This important body of work will be covered in Sec. VI B.

2. Chemical deposition

Chemical deposition processes are usually used when a lower thermal budget for the dielectric growth step is desired. Since deposition kinetics are slow at such temperatures (typically 350–600 °C), a plasma source is commonly used to activate the reaction. This technique has been used very effectively to deposit ultrathin Si–O–N with precise N distributions.[490,504–506] Chemical deposition methods do not consume the substrate, unlike thermal oxidation, and interfacial properties are usually inferior to those of thermal oxides. High temperature anneals ($\geqslant 750\,^{\circ}\text{C}$) are usually necessary to bring the electrical performance up to the level of thermal oxides.[490,491,507,508]

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

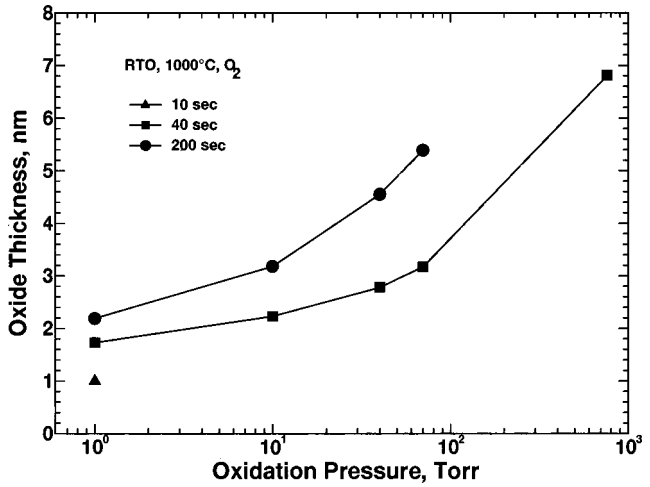


FIG. 72. SiO_2 thickness as a function of O_2 pressure for constant growth times. Layers were grown by rapid thermal oxidation at 1000 °C [M. L. Green (unpublished data)].

SiO_2 and Si–O–N layers have been deposited by chemical vapor deposition (CVD),[508,509] especially for the preparation of ''stacked'' oxide multilayers.[507] Such CVD/thermal oxide stacks may improve dielectric reliability.[510] However, their application to ultrathin gate dielectrics will be limited due to difficulties in controlling deposited layer thickness uniformity across large (200–300 mm) wafers. Thermal oxidation is inherently an easier process to implement uniformly. Atomic layer deposition (ALD), in which films are grown approximately one monolayer at a time, has been used to grow ultrathin SiO_2 layers.[511,512] This may be an important technique to grow $\leqslant 0.5$ nm SiO_2 layers, useful as buffer layers between Si and high-κ gate dielectrics. ALD has the outstanding advantages of superb conformal coverage as well as precise thickness control. Figure 74 illustrates one cycle of this layer-by-layer process. Jet vapor deposition (JVD) has been used to deposit high N-containing Si–O–N.[513,514] Although these layers have properties similar to Si_3N_4, the interface, and to a lesser extent the bulk, contain significant amounts of O. Gate dielectrics produced by this room temperature, supersonic gas flow, remote plasma technique are sufficiently intriguing to warrant further research.[515] Figure 75 is a schematic diagram of the JVD deposition scheme.

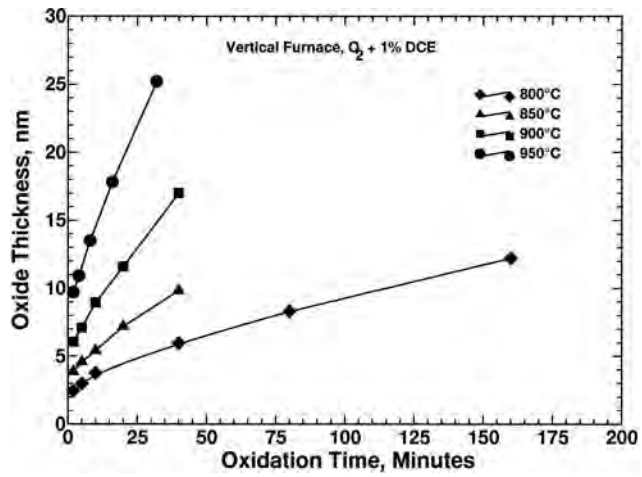


FIG. 73. SiO_2 thickness as a function of time, at various temperatures, for films grown in a vertical furnace at atmospheric pressure [M. L. Green (unpublished data)].

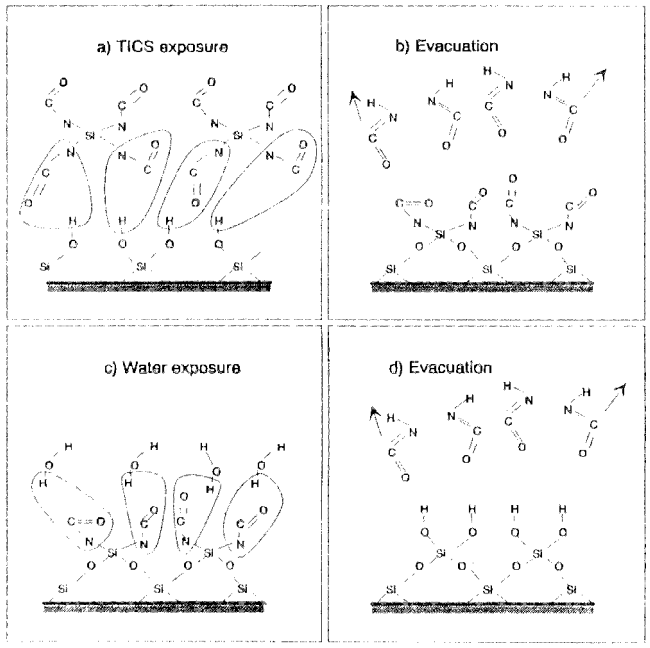


FIG. 74. Layer by layer (atomic layer) deposition mechanism of SiO_2 from tetraisocyanatesilane (TICS) and H_2O [from Gasser *et al.* (Ref. 511)].

Wet-chemically prepared oxides, e.g., the ultrathin (<1.0 nm) oxides resulting from chemical oxidation of the Si in oxidizing solutions ordinarily used to clean Si[461,516] or in H_2O[104] or ozonated solutions,[517] may be appropriate precursors for ultrathin gate dielectric layers. When annealed at temperatures as low as 350 °C they exhibit FTIR spectra identical to high temperature SiO_2.[104]

3. Physical deposition

Physical growth techniques for SiO_2 or Si–O–N include ion implantation, usually followed by an anneal or oxidation treatment, and high density plasma oxynitridation or nitridation. Both techniques afford great control over SiO_2 or Si–

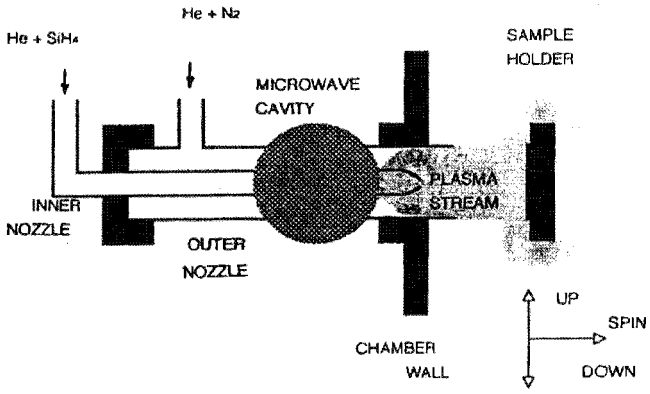


FIG. 75. Schematic diagram of apparatus for plasma assisted jet vapor deposition of Si_3N_4 from SiH_4 and N_2 [from Wang *et al.* (Ref. 513)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

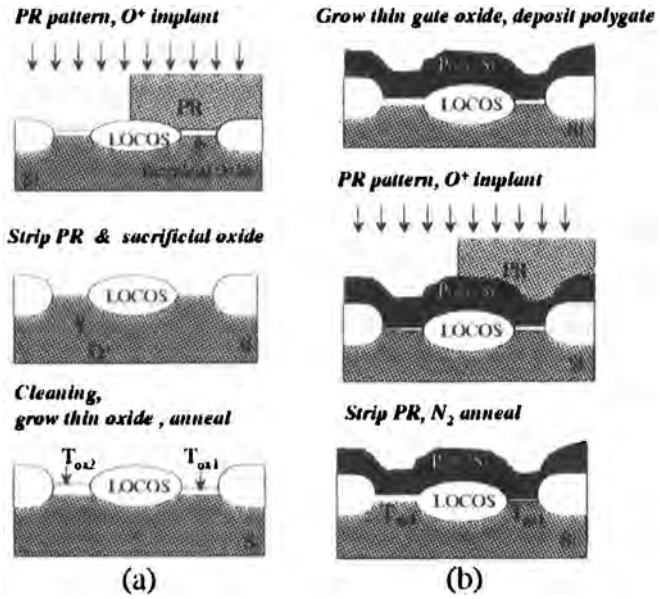


FIG. 76. Process flow for growing dual gate oxide thicknesses using an O preimplant [from King *et al.* (Ref. 68)].

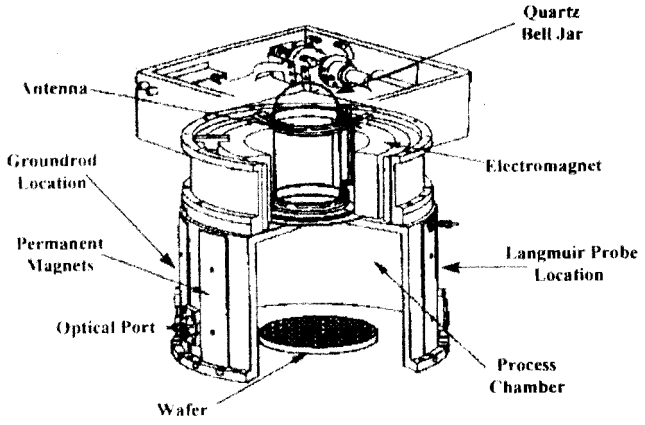


FIG. 77. Schematic of the process module for surface nitridation of SiO_2 in a high density N plasma [from Kraft *et al.* (Ref. 525)].

O–N thickness, composition, and structure. Using plasma nitridation, for example, one can incorporate much more N in an ultrathin layer than by thermal oxynitridation in NO or N_2O. Physical growth techniques are distinct from plasma or ion induced chemical deposition, in that in the former no deposition takes place. The dielectric layers are grown through the incorporation and subsequent reaction of the energetic species with the substrate. These techniques may induce damage in the substrate.

Conventional ion implantation has been used to grow ultrathin SiO_2,[68] Si–O–N,[518,519] and Si_3N_4.[520] Because it is desirable to have the implanted species close to the substrate surface to limit damage and facilitate subsequent incorporation during a high temperature step, the implantation should be done at low energies, for example <25 keV. Most conventional implanters do not afford high ion fluxes at these energies, so implantation time may become problematic for production. However, selective ion implantation is a unique scheme for growing dual oxide thicknesses on a single device, as is illustrated for the case of O implantation in Fig. 76. In this case the thicker oxide is created by the reoxidation of an area previously implanted with O. The same effect can be achieved by preimplanting N into selected areas.[67] Most of the implanted N is incorporated into the growing Si–O–N during subsequent oxidation; the retarding effect of incorporated N on oxidation kinetics[519,521] is utilized to result in a thinner oxide in the N implanted areas. Although these schemes are very attractive from a device design standpoint, it remains to be seen if the implanted SiO_2 and Si–O–N films have the required reliability for ULSI devices.[522] Finally, Si–O–N films have been grown by implantation of NO^+ to directly form Si–O–N.[523] Thus far this method has not been applied to ultrathin films.

Plasma immersion implantation is a high ion flux rate technique that allows rapid incorporation of the implanted species at low energies. Thus ultrathin layers can be grown without the time constraint of conventional implantation. However, there is no mass selectivity using this method, and other species present in the chamber may be extracted from the plasma and implanted as well. For example, since H_2O is ubiquitous in many plasma chambers, Si–O–N films usually result from growth in a nominal N plasma.[524] Since N ions may be extracted from the plasma at very low energies, i.e., the floating potential of ~ 10 V, very shallow implantation is possible. Thus the surface of previously grown thermal oxides can be lightly implanted with N[525] using, for example, the apparatus depicted in Fig. 77. Unlike incorporation of N during thermal oxynitridation in NO or N_2O, where the N is confined to the Si/SiO_2 interface, mobility degradation is not observed with the plasma process because the N is at the SiO_2 surface.[526] In addition, reliability of these oxides is acceptable, in spite of the damage caused by the plasma implantation, if proper annealing treatments are used.[527] However, for the case of sub-2.0 nm plasma immersion oxides, both mobility and reliability may be degraded. Further studies of plasma immersion nitridation have been carried out.[528–530] Higher temperature favors nitridation, over oxidation caused by residual species such as H_2O, and compositions closer to Si_3N_4 are possible.[531,532]

C. Postoxidation processing and annealing

Crucial electrical performance parameters such as mobility and interface state density are directly related to physical structure and chemical bonding at the Si/SiO_2 interface. This interface does not reach its final configuration after oxidation, but rather after all postoxidation processing has been completed.[486] Since the interface is defined by the last SiO_2 to form and the last thermal and/or physical (e.g., irradiation) treatment it is exposed to, postoxidation processing, which involves among other steps implant activation annealing, polycrystalline Si deposition, and plasma etching and deposition, greatly impacts the properties of the gate dielectric. Plasma processing in particular has been studied as a major issue in determining the final electrical quality of gate dielectrics.[533–535]

A fundamental understanding of the ''processing window'' for postoxidation treatments is absent, making the pos-

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

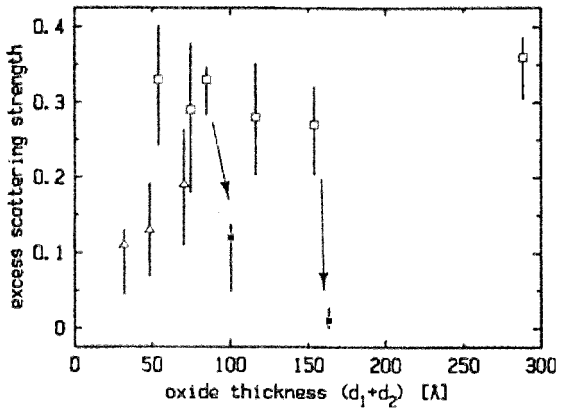


FIG. 78. Excess scattering strength in the interfacial layer, as measured by x-ray reflectometry, as a function of oxide thickness. The open squares correspond to as-grown layers grown in 760 Torr of O_2, and the open triangles for layers grown in 40 Torr of O_2. Annealed layers are indicated by the closed squares. Annealing is seen to remove the high density interfacial layer, since the excess scattering decreases [from Kosowsky *et al.* (Ref. 184)].

toxidation arena a fertile area for research. It is generally agreed that annealing parameters play an important role in device manufacturing.[536] However, in most cases these parameters are chosen empirically and not optimized. For example, the transition region at the Si/SiO_2 interface has been studied in great detail (see Sec. V). It has been suggested that high temperature annealing after oxidation will minimize the high density transition layer and result in improved electrical performance.[184,537,538] X-ray reflectivity has been used to study the effects of annealing on the transition layer, as is shown in Fig. 78. Spectroscopic ellipsometry has also been used to study SiO_2 density changes as a function of oxidation temperature and postoxidation annealing parameters.[539] Higher temperature growth or annealing was seen to reduce SiO_2 density.

Several postoxidation annealing studies have concerned themselves with interfacial roughness. *In situ* TEM studies of the interface have shown that postoxidation annealing improves roughness for the (100), but not the (111) interface.[540] TEM, STM, and electrical measurements have been correlated in another study, in which it was found that annealing in Ar improved roughness for low index [e.g., (100) or (110)] interfaces, but degraded higher index interfaces.[541] Spectroscopic ellipsometry has been used to show that roughness is reduced by reoxidation of suboxides at lower temperatures ($<$900 °C), and by viscous flow at higher temperatures.[75] Longer anneals have been shown, through EPR studies, to result in irreversible degradation of the interface due to formation of silicon monoxide, SiO.[542,543]

D. Hydrogen/deuterium processing

It has long been realized that H plays an important role in MOS device performance.[21,33,225,543–551] The relatively high background level of H-containing molecules in silicon microelectronics processing ambients (e.g., NH_3 and SiH_4 in CVD reactors), and the high diffusivity of H in SiO_2, supports the belief that H is ubiquitous in the Si/SiO_2 system.[544,552–556] In fact, nuclear reaction analysis experiments have revealed that H[557] or D[220] concentrations in SiO_2 films can be as high as the 10^{21} cm^{-3} range. Figure 79 shows D depth profiles for a thin ($\sim$5 nm) SiO_2 film annealed in D at 450 °C.[220,221] One can see that D is located in an extended region close to the interface.

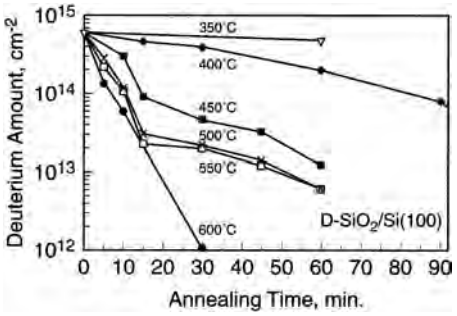


FIG. 79. Integrated amount of D, measured by nuclear reaction analysis, in a thin ($\sim$5.5 nm) deuterated SiO_2 film, as a function of vacuum annealing temperature and time [from Baumvol *et al.* (Ref. 221)].

Hydrogen, as well as D, in their many bonding and isotopic configurations including atomic/molecular H, $Si–H^+$, OH groups, and bridging H, influence the electrical behavior of the Si/SiO_2 system through various defect processes, as can be seen in Fig. 80.[64,65,404,453,549] Hydrogen annealing below $\sim$600 °C has been proven to passivate dangling bonds at the interface, which in turn further reduces the concentration of surface states.[33,544,546,550] On the other hand, it has been demonstrated that H can be associated with detrimental effects such as negative-bias-temperature instability (NBTI), radiation induced interface traps and oxide charges, and depassivation of interface traps in MOS-based devices.[546,550,555,558,559] The role of atomic H has been specifically pointed out in many of these effects.[64,549,558–560] Recent first principles density functional calculations suggest that SILC in MOSFETs with ultrathin oxides can be attributed to the H bridge, a complex between an O vacancy and a H atom in which the H atom occupies the bond center of a Si–Si bond, similar to interstitial H in SiO_2.[561] In addition to the electrical effects, H may be involved in chemical reactions in the SiO_2 films, such as oxidation in nominally dry and wet ambients, and nitridation via the use of NH_3,[218]

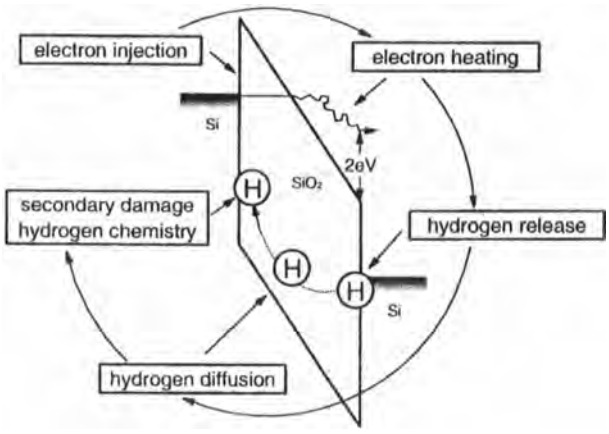


FIG. 80. Schematic energy band diagram showing defect generation processes in the Si/SiO_2 system involving H [from Stathis *et al.* (Ref. 750)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

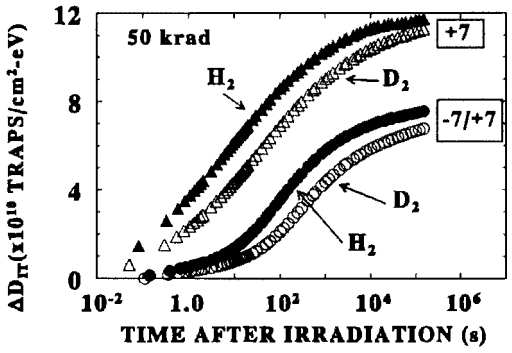


FIG. 81. Increase in the density of interface traps (D_{it}) as a function of time, after 40 MeV electron irradiation, for metal–oxide–semiconductor structures annealed in D_2 or H_2 for two bias protocols: (i) 7 V or (ii) −7 V during irradiation, then switched to 7 V [from Saks *et al.* (Ref. 566)].

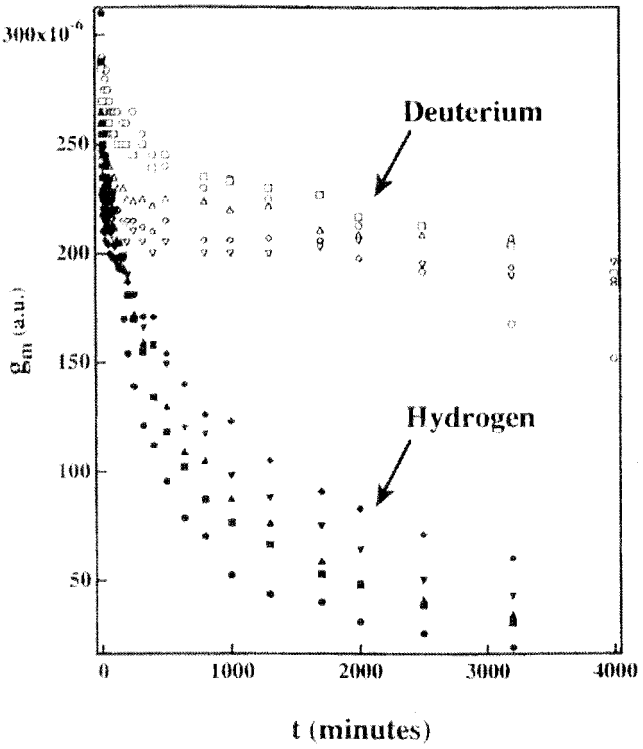


FIG. 82. Time dependent degradation of the transconductance (g_m) for five N metal–oxide–semiconductor transistors annealed at 400 °C for 1 h in H_2 or D_2 [from Lyding *et al.* (Ref. 567)].

although this mechanism is not well-understood.[37] More details on the behavior of H in the Si/SiO_2 system can be found in recent review papers.[543,544,546,547] Hydrogen also plays an important role in thin Si_3N_4 and Si–O–N films deposited on Si, as summarized in recent reviews.[37,225,506]

Replacing H by its heavier isotope, D, offers advantages both for studying fundamental aspects of H/D behavior in ultrathin SiO_2 films, as well as for improving the electrical properties of the devices. Several groups have successfully used D to mimic basic aspects of H reactivity and diffusivity in SiO_2.[220,229,231,562–565] The practical benefits of D processing include improved immunity of the D-passivated Si/SiO_2 interface against electrical stressing.[565–575] In particular, D annealed MOSFETs showed a retardation of the rate of interface trap buildup, under gamma irradiation, by factors of 2.6–4.5 compared to conventional H processing,[566] Fig. 81. Lyding and coworkers demonstrated that final annealing of NMOS devices in D, instead of H, resulted in improved hot electron degradation immunity,[567,571,575] as is shown in Fig. 82. It was further observed that the hot electron reliability lifetime of transistors was improved by factors of 10–50,[571] Fig. 83. Subsequently, the D isotope effect was confirmed by other groups,[568,569,572,573,576] Fig. 84.

It is clear that the difference in mass between H and D is not enough to explain the significant isotopic effects. Electronic effects also need to be taken into account.[571,577] One can draw an analogy between the electrical findings and results of experiments on H and D desorption from Si surfaces induced by tunneling current from an STM tip, Fig. 85, in which a large isotopic effect was observed.[571,578] It was argued that H and D desorption from the interface under hot electron electrical stress can be caused by multiple excitations of the Si–H or Si–D vibrational modes. The desorption yield is governed by competing processes: the excitation rate, which in turn depends on current density and electron energy, and the excitation decay via substrate phonons. It was postulated and then deduced from first principles calculations that the coupling between the substrate phonon modes and Si–H and Si–D vibrations is much stronger for the Si–D case.[571] This enables more efficient energy dissipation of the excited Si–D bond, whereas in the Si–H case it is easier to pump the energy up until the bond breaks. As a

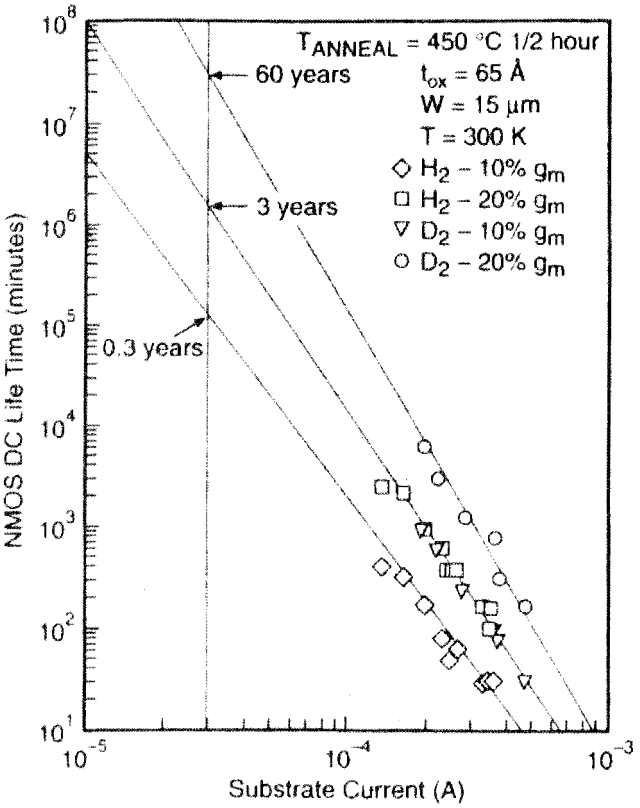


FIG. 83. Hot electron degradation lifetime versus substrate current, under stress voltages of 4.2–4.6 V, for transistors annealed in H_2 or D_2 [from Hess *et al.* (Ref. 571)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

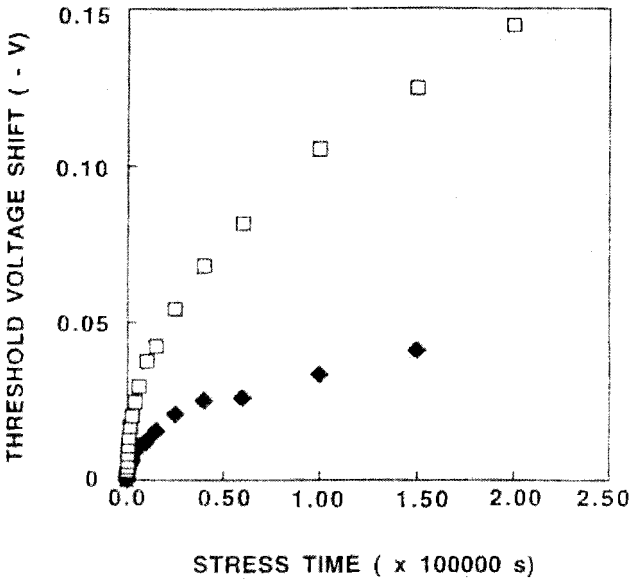


FIG. 84. Threshold voltage shift as a function of hot electron stress time for transistors annealed in H_2 (open symbols) or D_2 (closed symbols) [from Devine *et al.* (Ref. 568)].

result, the D at the interface exhibits much longer lifetime under electron stressing, as was seen in Fig. 83. One model of hot electron degradation, alluded to above, invokes H desorption during excitation. Further elucidation of this point requires an understanding not only of all relevant bulk and H-defect vibrational frequencies, but also direct measurements of the vibrational lifetimes of the Si–H and Si–D modes themselves. Ultrafast optical experiments offer direct evidence for the lifetimes, thereby significantly increasing our understanding of H/D effects in defective solids. Recent bulk studies, combined with previous work on surfaces, is leading to a much deeper understanding not only of vibrational lifetimes, but more importantly of MOSFET transconductance degradation.[579]

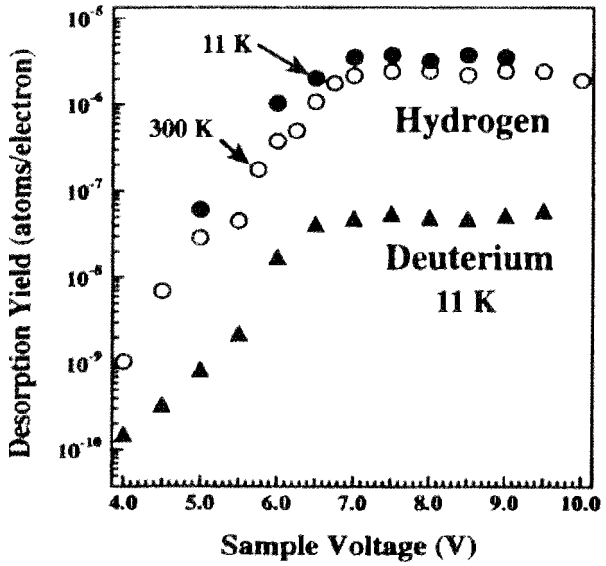


FIG. 85. The yields of H and D desorption from the Si surface in the electronic excitation regime, as a function of voltage, determined from low temperature scanning tunneling microscopy measurements [from Foley *et al.* (Ref. 578)].

The isotopic effect is very sensitive to processing history, especially to the way the D is incorporated into the gate dielectric, and subsequent thermal processing. The magnitude of the effect seems to be correlated with the amount of D left after all processing steps.[571–573] Deuterium anneals in the 400–600 °C range are usually used to dose the gate dielectric and the interface with D, as can be seen from Fig. 79. The amount of incorporated D is strongly dependent on the materials structure of the device. Deuterium diffuses easily through SiO_2 layers, whereas Si_3N_4 layers significantly retard D penetration.[569,580] It is also observed that impurities, for example dopants in polycrystalline Si gate layers, may affect the diffusivity, since undoped polycrystalline Si appears to be an efficient barrier for D transport.[580] Ference and coworkers employed a deuterated PECVD Si_3N_4 capping layer for the MOSFETs, both as a huge reservoir of D close to the gate, as well as an efficient diffusion barrier to prevent its escape under subsequent thermal treatment, and observed a significant effect on hot electron immunity.[572,573] As far as the thermal anneals are concerned, one can see from Fig. 79 that D in SiO_2, like H, is not very stable and tends to escape at temperatures higher than approximately 550–600 °C.[221,550,581]

V. THE Si/SiO_2 SYSTEM

A. The initial stages of oxygen interaction with silicon surfaces

The interaction of O with the Si surface is known to depend on temperature, time, and O_2 pressure.[26–29,147,268,289,300,301,582–585] Lander and Morrison,[586] and subsequently others,[268,281,294,301,582,587–592] observed two distinct regions in pressure-temperature phase space, Fig. 86, that represent completely different O–Si interactions. In the low temperature-high pressure half of the diagram, O interaction with the surface results in oxide growth:

$$\mathrm{Si}(s)+\mathrm{O_2}(g)=\mathrm{SiO_2}(s). \tag{11}$$

In the high temperature-low pressure regime, on the other hand, surface etching via volatile SiO formation, also known as disproportionation, occurs:

$$2\mathrm{Si}(s)+\mathrm{O_2}(g)=2\mathrm{SiO}(g). \tag{12}$$

These oxide growth and etching modes are often referred to as ''passive'' and ''active'' oxidation, respectively. Recently, several groups have shown that there is a transition regime in pressure-temperature space between the active and passive oxidation modes (also shown in Fig. 86), where the surface morphology differs dramatically from that of either region.[268,281,301,587,591] In particular, it has been shown that the surface becomes very rough in this region, as is shown in Fig. 87, whereas under normal active and passive oxidation the surface may remain flat, Fig. 88. Below, we summarize the critical aspects of the interaction of O with Si surfaces. More details on O adsorption and the initial stages of Si oxidation may be found elsewhere.[26]

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

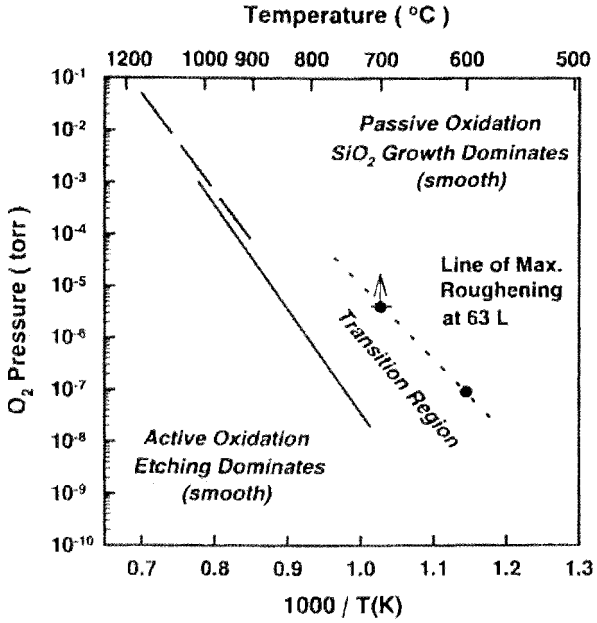


FIG. 86. Oxygen pressure-temperature phase diagram for Si(100) showing three different oxidation regimes. The transition (roughening) regime was deduced from scanning tunneling microscopy measurements of surface roughness [from Seiple *et al.* (Ref. 281)]. The solid and the dashed lines are from Lander *et al.* (Ref. 586) and Smith *et al.* (Ref. 582), respectively.

1. The passive oxidation regime

Basic questions about the first few monolayers of oxide growth, such as whether the initial oxidation proceeds by a layer-by-layer or three-dimensional island growth mechanism, have been intensely debated over the past decade.[26,147,268] Research tools brought to bear on this problem include conventional XPS,[146,147,156,583] synchrotron-based XPS,[130,159,593] HRTEM,[261,262] LEEM,[272] and MEIS.[199,204] Further, STM results for submonolayer O coverages have been reported.[284,285,289,290,300,301,587,594–596]

Some STM images show nucleation and growth of oxide islands on Si(111)[285,290,301,594,595] and Si(100)[287,289,294,587] surfaces, as is illustrated in Fig. 89. The islands are thought to be one monolayer high. However, since STM sees a local density of states at the surface rather than a real geometrical map of surface atoms, changes in the local electronic configuration of the Si and O atoms must be considered when interpreting STM images. For example, in one report the difference in grayscale level in the images, Fig. 89, was argued to represent different height variations (0.2 nm) in oxide islands grown at 873 K.[290] However, larger contrast variations, observed for a higher temperature oxide, could easily be due to a change in the local electronic configuration, e.g., local stoichiometry, rather than a simple height variation.

Island growth was also suggested from both core level and valence band photoemission experiments.[149,159,597] These studies show nonuniform oxidation behavior at submonolayer coverages, with phase separation of oxidized and nonoxidized areas on the surface, as seen in Fig. 89. Oxidation kinetics at high temperatures was also described within a nucleation and growth model,[147] and island growth of the surface oxide has been predicted from first principles calculations.[598,599] Some researchers suggested that oxide island growth at elevated temperatures proceeds via surface diffusion of O to the growing oxide islands.[147,290] However, relatively little is known about O diffusivity on Si surfaces.[278] STM studies have suggested that O diffusion actually occurs as SiO bound to the surface, which is chemically reasonable given the known stability of SiO. We also note that STM images taken during the interaction of O with Si at room temperature show a more uniform O overlayer in comparison to those taken after elevated temperature anneals,[285,287,290] offering further evidence for the thermodynamic stability of SiO_x islands. Photoemission, scanning tunneling spectroscopy, and EELS experiments are consistent with the interpretation that the stable bonding configuration for O at submonolayer coverages is the bridging position between two Si atoms.[122,129,159,161,285,290,600–602] Some alternative metastable structural models have been suggested for surface bound O, notably singly bound O with a dangling

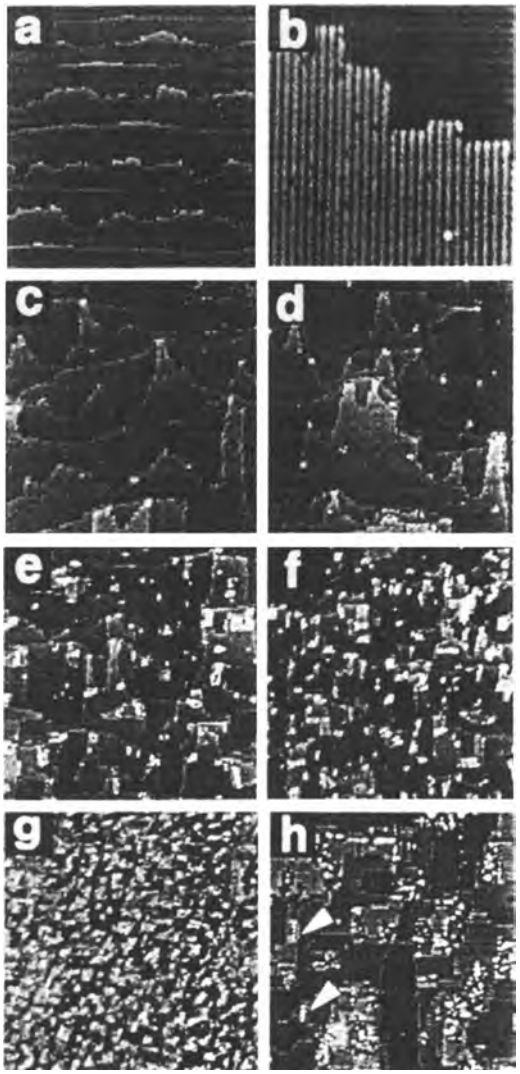


FIG. 87. Large area (300×300 nm^2) scanning tunneling microscopy topographs of the initial Si(100) surface (a) [a 20×20 nm^2 closeup of which is shown in (b)], and after exposure to increasing O pressure from (c) 2×10^{-8} Torr to (h) 1×10^{-7} Torr. For all figures (c)–(h) the total O exposure was 63 L [from Seiple *et al.* (Ref. 587)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

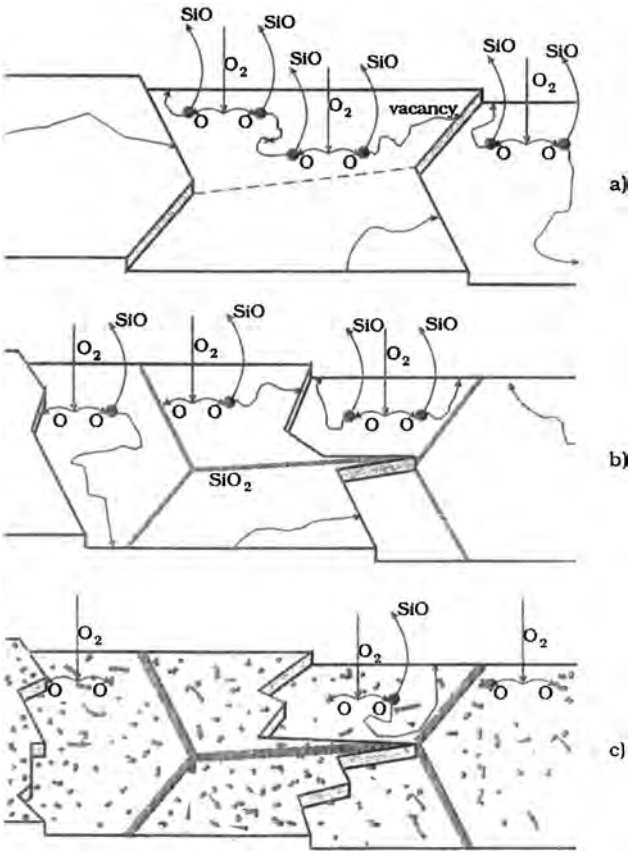


FIG. 88. Schematic representation of the three different mechanisms active during the interaction of O with Si surfaces at high temperatures: (a) active oxidation (SiO desorption), (b) roughening regime, and (c) passive oxidation (SiO_2 growth) [from Feltz *et al.* (Ref. 301)].

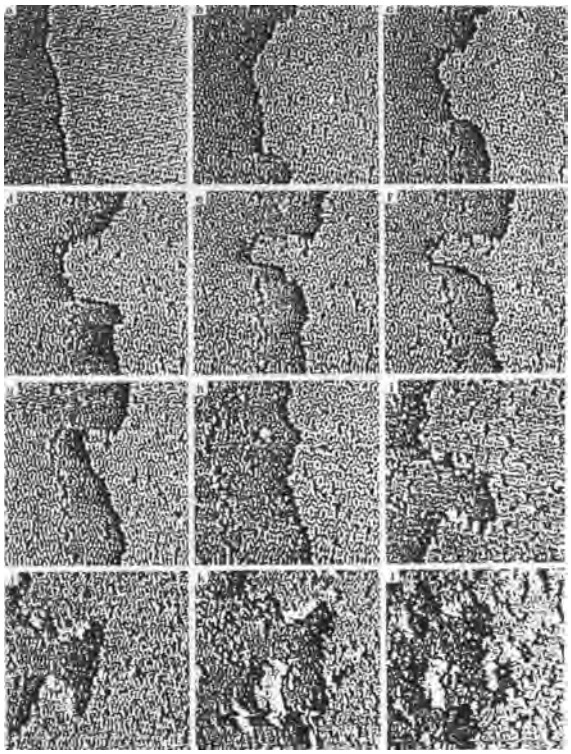


FIG. 89. Series of scanning tunneling microscopy images (36×36 nm^2) during Si(111) passive oxidation (850 K, 1×10^{-6} Pa) as a function of time: (a) clean Si(111) 7×7 surface to (1) 1205 second exposure. Inhomogeneous oxide nucleation at steps and homogeneous oxide nucleation on terraces can be seen [from Feltz *et al.* (Ref. 301)].

bond, peroxy Si–O–O–Si species, and singly bound O_2 species.[104,272,312,603,604]

Oxidation behavior, after the first monolayer, has been studied by XPS, AFM, TEM, SREM, and MEIS. Stepwise evolution of the net concentration of Si^{n+} ($n=1,2,3,4$) oxidation states, as measured by Si $2p$ XPS during the oxidation of Si(100),[159] Fig. 90, and antiphase oscillations of Si^{1+} and Si^{3+} intensities as a function of oxide thickness on Si(111),[156] Fig. 91, were cited as support for layer-by-layer oxidation. [Although the term ''layer-by-layer growth'' has become popular in the literature to describe the initial oxidation of Si, one should keep in mind that, (i) thermally grown SiO_2 on Si surfaces is amorphous and, therefore, not a layered system, and (ii) traditionally this term refers to thermodynamically stable structural behavior during film growth (i.e., the Frank/van deer Merwe growth mode), whereas the initial oxidation of Si is likely kinetically limited, at least under some conditions.] In contrast, XPS results[130] were interpreted as implying discontinuous, island-like film growth for oxide thicknesses less than 0.8 nm.

When interpreting XPS results, one should keep in mind that experimental data are subject to different interpretations and analyses. An analysis of XPS (Al $K\alpha$, 1487 eV) and synchrotron XPS (130 eV) data taken on the same $Si(100)/SiO_2$ sample yielded differences in the concentration of the Si^{n+} states by as much as a factor of 2, and a difference of about 30% in the oxide thickness.[134] This discrepancy was attributed to differences in data analysis caused by uncertainties in cross sections, photoelectron mean free paths, and takeoff angles, rather than fundamental differences between the two techniques. Other XPS[146] and synchrotron XPS[593] experiments performed on samples oxidized under similar conditions also yield different results. In addition, the traditional interpretation of the Si^{n+} suboxide states observed in photoemission, Fig. 18, as a Si atom with n ($n=1,2,3$) O bonds in the first coordination sphere,[122,124,125,130,161] is currently under debate.[133,136,165,167,605] An alternate interpretation derives from experiments illustrated in Fig. 19. It has been argued that the local electronic configurations, and corresponding Si $2p$ chemical shifts, around each Si atom depend not only on the nearest neighbor configuration but also on the O–Si bonding in the second coordination sphere.[133,136,166,167] Two different first principles electronic structure calculations support the traditional interpretation of the Si $2p$ photoemission spectra, but differ as far as the second nearest neighbor effects are concerned.[163–165,605]

Hattori and colleagues[144] used *in situ* noncontact mode AFM to examine the evolution of SiO_2 surface microroughness during the initial oxidation of Si(100) and Si(111). It was observed that the surface roughness varies periodically with the progress of oxidation, Fig. 92. The change of the microroughness was found to correlate with periodic oscillations of the XPS signal, illustrated in Fig. 91, of the suboxide states, in particular Si^{1+}. This observation was interpreted in

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

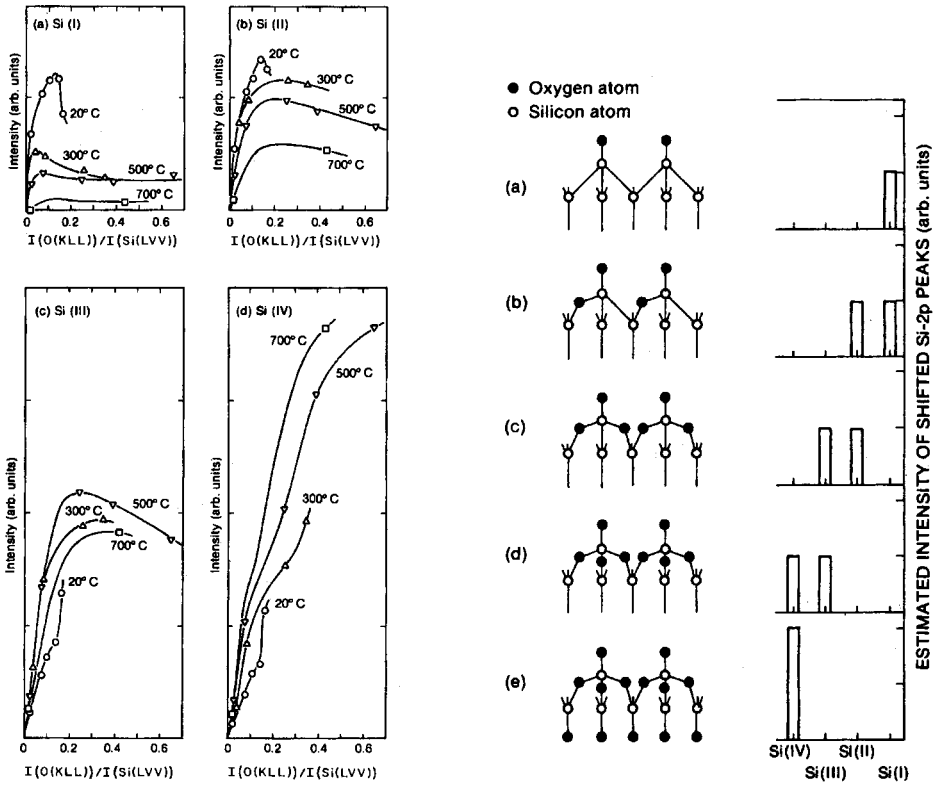


FIG. 90. (Left) Peak heights of the Si^{1+}, Si^{2+}, Si^{3+}, and Si^{4+} oxidation states [measured by synchrotron based photoelectron spectroscopy during the initial oxidation of Si(111) at different temperatures] as a function of O coverage, measured by Auger spectroscopy. The right panel shows possible bonding configurations and corresponding peak intensities. One can see that at room temperature all Si atoms are oxidized at more or less the same rate, whereas at high temperatures some Si atoms are oxidized faster. The distribution of adsorbed O is therefore highly nonuniform [from Tabe *et al.* (Ref. 159)].

terms of the formation of Si^{1+} at the interface which, in turn, causes the formation of protrusions at the oxide surface, Fig. 93, further supporting the layer-by-layer model of growth.[144]

Surface composition and morphology on Si(111) have been studied by MEIS for passive oxidation conditions.[591] It was shown, Fig. 94, that the width of the O backscattering peak, as a function of O coverage at elevated temperatures, has a plateau for coverage less than 3.2 ± 0.4 monolayers. This result is consistent with a model in which the surface is covered by a nonstoichiometric oxide before ''bulk'' oxidation begins. As oxidation proceeds the O peak broadens, reflecting oxide growth in the subsurface layers.[591] Surface oxide formation at elevated temperatures was compared with the interaction of O with Si at 300 K. These results imply that the difference in oxidation between elevated and room temperatures is due to a difference in local stoichiometry.

One can distinguish between two different kinds of layer-by-layer oxidation. The first refers to a single atomic layer being oxidized at a time, which can be called monolayer growth. A second case refers to a bilayer growth mode, with the unit being a Si bilayer. Ross and coworkers[266,268] showed, via real-time HRTEM experiments, that surface

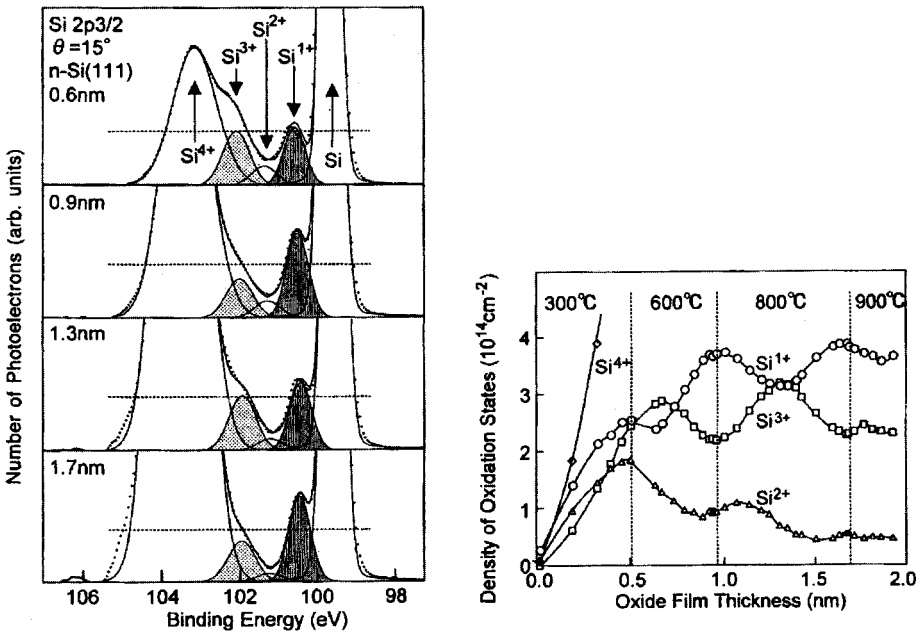


FIG. 91. (Left) Si $2p$ photoelectron spectra showing the evolution of the Si^{1+}, Si^{2+}, and Si^{3+} suboxide states during the initial oxidation of Si(111). The right panel summarizes the density of the suboxide states as a function of oxide thickness [from Ohishi *et al.* (Ref. 156)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

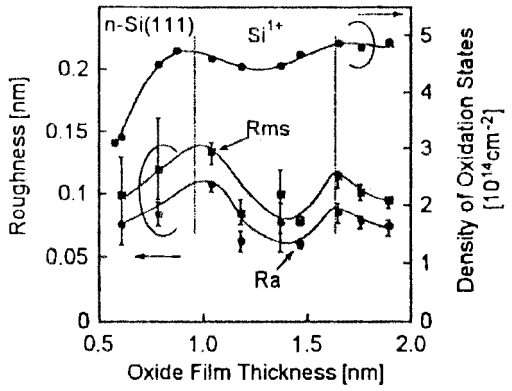


FIG. 92. Changes of the root mean square (determined by atomic force microscopy) value of surface roughness and the Si^{1+} suboxide states during initial oxidation of Si(111) [from Hattori *et al.* (Ref. 144)].

steps are immobile during the initial oxidation of Si(111), suggesting that the oxidation follows a monolayer growth mode, depicted in Fig. 38. Photoemission results, Fig. 91, also imply a monolayer growth mode.[144]

The kinetics of the initial oxidation of the Si(001) surface was recently explored by SREM, in combination with Auger measurements of O and Si signals.[271] Very similar to the pioneering microscopy work by Ross and Gibson,[267,268] a periodic reversal of the SREM contrast and immobility of the surface steps was observed, as can be seen in Fig. 39. Based on these observations, the authors concluded that the most likely layer-by-layer oxidation scenario is random nucleation of nanometer-scale oxide islands, followed by their subsequent lateral growth.

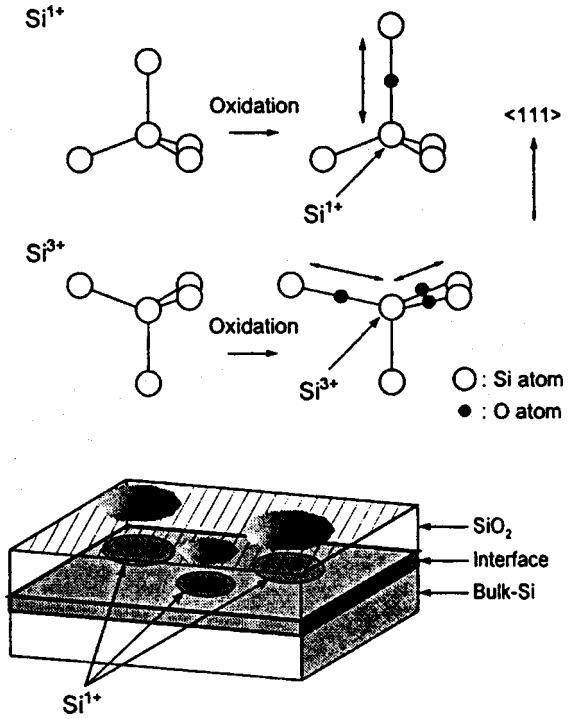


FIG. 93. Schematic model illustrating the correlation between the periodic oscillations of surface roughness and the Si^{1+} suboxide states during the initial oxidation of Si(111) as evidenced in Fig. 92 [from Hattori *et al.* (Ref. 144)].

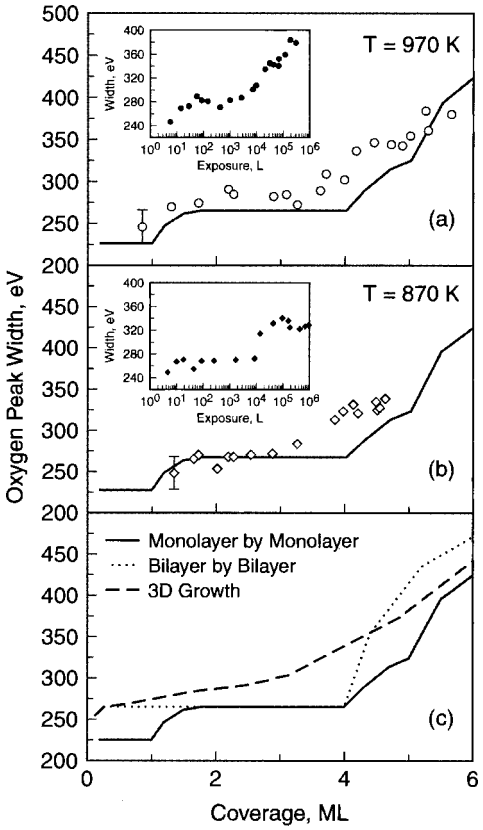


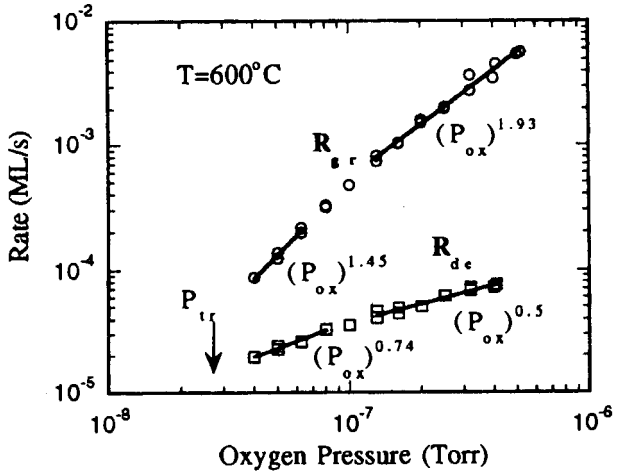
FIG. 94. Medium energy ion scattering studies of the interaction of O with Si(111). The plots show how the width of the O MEIS peak (which is a measure of the oxide layer thickness) changes as a function of O coverage (1 monolayer=7.8×10^{14} O/cm^2) and O exposure (in the insets). The bottom panel shows simulation results for three different growth modes [from Lu *et al.* (Ref. 591)].

Shklyaev *et al.*[588,589,606] used optical methods, including ellipsometry and second harmonic generation, to study the very early stages of oxide formation as a function of pressure, temperature, and ambient (O_2 vs N_2O). A decrease in the rate of oxide formation was observed with decreasing oxidant pressure as the transition to the Si etching regime is approached, shown in Fig. 95. These results were interpreted with an oxide island nucleation and growth model, according to which the nucleation proceeds through the interaction of the layer of intermediately adsorbed species, with the critical size of the islands decreasing with O pressure.

Infrared absorption spectroscopy and density functional cluster calculations were recently used to study the initial oxidation of Si using the H_2O-exposed Si(100)-(2×1) surface as a model.[104,607] The Si–Si dimer bond was found to dissociate during initial oxidation, followed by O incorporation into the Si backbonds. It was also found that high temperature annealing of this surface results in the formation of Si-epoxide intermediate states, consisting of three-membered Si–O–Si rings.[104]

Finally, we should mention the change of the electronic band gap of ultrathin SiO_2 layers on Si as a function of oxidation, as observed by valence band spectroscopy.[143,144] One can see that while for thicker films the band offset does not change with thickness, Fig. 96, for thinner films the top of the SiO_2 valence band decreases by approximately 0.2 eV

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp



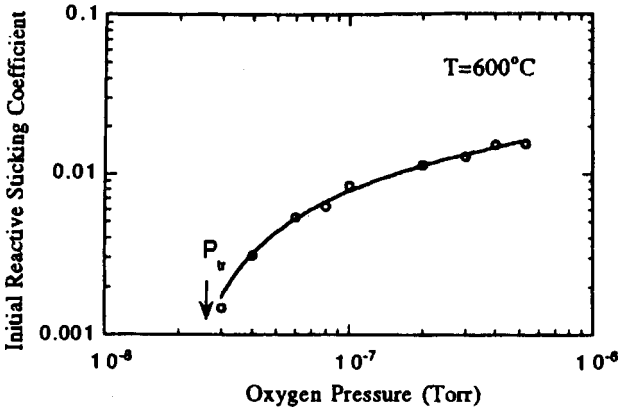


FIG. 95. Pressure dependence of the initial growth rate (R_{gr}) and oxide decomposition rate (R_{dc}) (upper panel), and the initial sticking coefficient (lower panel) [from Shklyaev (Ref. 606)].

as the films become thicker than ~0.9 nm, Fig. 97. This result is consistent with local density cluster calculations of ultrathin SiO_2 layers, in which it was found that the band gap decreases for films thinner than 0.7 nm.[608] Muller and coworkers used STEM to study the physical and electronic structure of ultrathin SiO_2 layers[17] and recently followed this up with *ab initio* electronic structure calculations.[609] Muller's results, Fig. 6, have been interpreted to show that more than a monolayer of Si at both interfaces of a $Si/SiO_2/Si$ sandwich are in the suboxide configuration, and that this suboxide has wave function tails that decay slowly into the SiO_2. The result of this analysis places limitations on how thin such a structure can be and still limit charge transport to acceptable levels in devices. Although the concept of a scaling limit for SiO_2 films, in the range 1 to 2 nm, is agreed upon by most workers in the field, the authors' provocative interpretation of their STEM data has yet to be substantiated by other methods.

2. The active oxidation regime

Walkup and Raider[610] used laser induced fluorescence to study SiO(g) evolution during O interaction with Si(111). SiO molecules were detected in the active oxidation regime.

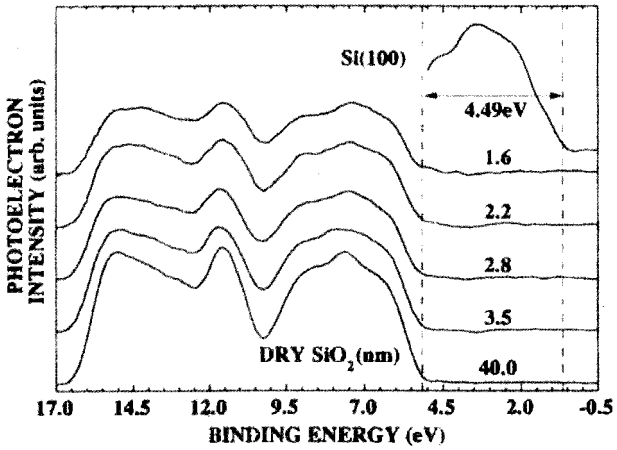


FIG. 96. Valence band density of states for ultrathin dry oxides of thicknesses of 1.6–40 nm [from Alay *et al.* (Ref. 143)].

On the other hand, they noted that in the passive oxidation regime, the SiO density in the gas phase was below the detection limit, 3×10^6 molecules/cm^3. SiO desorption was found to be thermally activated and linearly dependent on the O flux (pressure). SiO evaporation under active oxidation conditions was also observed using mass spectrometry.[27] Starodub and coworkers[592] developed a sensitive XPS method for detecting volatile SiO species, based on its condensation on an Ag foil. As an example, Fig. 98 shows how SiO desorption increases with temperature (the amount of Si condensed on the Ag foil is proportional to the area under the Si $2s$ XPS peak). They also found that small but measurable yields of SiO(g) desorb from the oxide film during the initial stages of passive oxidation, even when the oxide film continuously covers the surface.

SiO desorption implies that Si atoms leave the surface, i.e., that surface etching is occurring. Surface etching has also been observed as a result of Si interaction with other reactive gases, for example, I[611] and Cl,[477,612] at high temperatures. Surface morphology in this oxidation regime has been studied by conventional electron microscopy in the

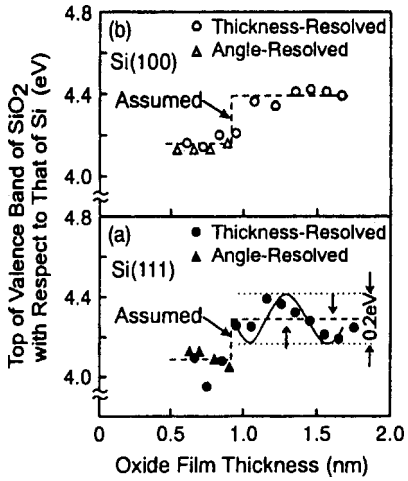


FIG. 97. Changes in the top of the valence band edge of ultrathin (<1.6 nm) oxide films grown on Si(100) and (111) surfaces [from Hattori *et al.* (Ref. 144)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

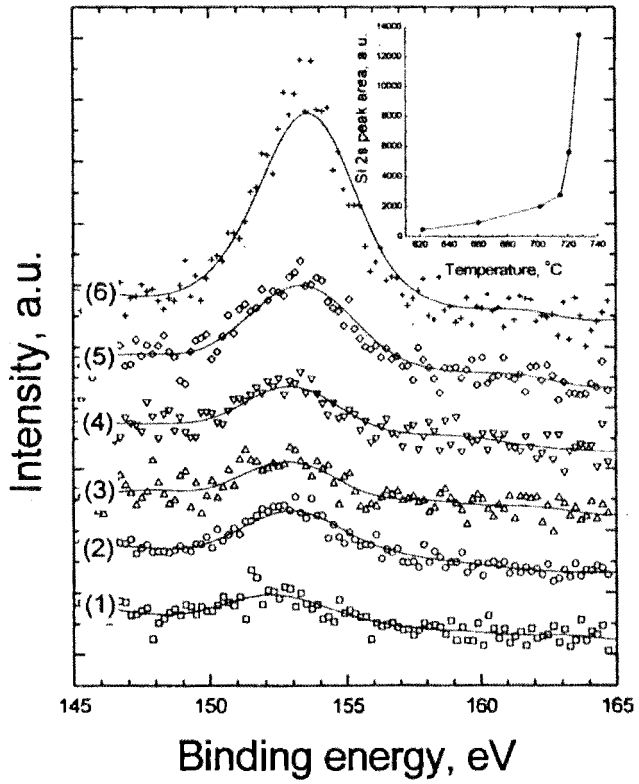


FIG. 98. Si 2*s* photoelectron spectra for SiO deposited on a cold Ag surface (placed just above the Si wafer) during the first 10 min of oxidation of Si(100) at a pressure of 10^{-7} Torr and at different temperatures: (1) 620 °C, (2) 660 °C, (3) 700 °C, (4) 715 °C, (5) 720 °C, and (6) 728 °C. The inset shows the temperature dependence of the area under the Si 2*s* peak [from Starodub *et al.* (Ref. 592)].

reflection[254,613] and transmission[266,268] modes, by LEEM[272], and by STM[294,301]. It has been shown[254,268,301,613] that etching in the ''pure'' active oxidation regime at high temperatures proceeds via a step-flow mechanism for both Si(111), Fig. 38, and Si(100), Fig. 39. Both the step velocity and the ''vertical'' etch rate increase with O_2 pressure and appear to be independent of the substrate temperature. The origin of the step movement across the surface has been explained in two different ways. Ross *et al.*[268] suggested that the step flow is caused by preferential evaporation from step edges with O diffusion to the step. However, Feltz *et al.*,[301] using AES, did not detect O on the surface and argued, therefore, against this mechanism. They and other workers favor a model where the step flow is caused by the formation of surface vacancies, taking place uniformly over the surface terraces, with their subsequent diffusion to the steps.[254,272,301]

Vacancy diffusion to, and disappearance at steps gives rise to step movement across the surface. The vacancy diffusivity has been shown to be much higher than the surface mobility of O.[301] For the Si(100)-(2×1) surface, the diffusing species is believed to be a divacancy, preferentially diffusing along the dimer rows.[272] The surface vacancy diffusion length and terrace width are important factors that affect surface morphology during active oxidation. If the diffusion length is greater than the terrace width, only step etching occurs. At the opposite extreme, surface vacancies can form an island or a two-dimensional vacancy hole, as observed

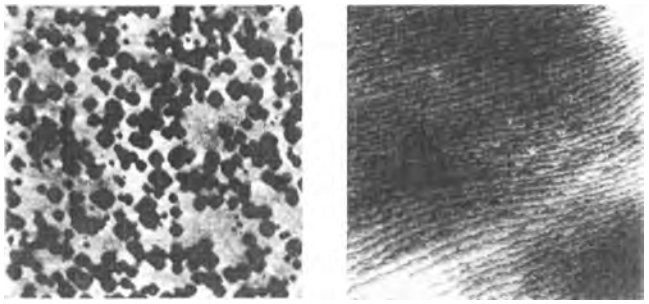


FIG. 99. Left: 10×10 μm^2 atomic force microscopy image of Si(100) with a native oxide that has been partially desorbed by annealing at 780 °C for 30 min. A high density of voids (100–500 nm wide, 4 nm deep) is seen on the surface. Right: 1×1 μm^2 scanning tunneling microscopy image of a smooth Si(100) surface after desorption of native oxide at 780 °C for 10 min with a Si flux of ~0.1 nm/s [from Wilk *et al.* (Ref. 283)].

experimentally by REM, STM, and LEEM.[254,272,301] Vacancy island formation processes during active oxidation are similar to nucleation and growth of surface holes during Si sublimation at high temperatures[254,269,614] and during low energy ion bombardment at high temperatures.[615–617]

The fact that SiO desorbs under high temperature-low pressure conditions can be used for *in situ* precleaning of Si wafers covered with ultrathin native, chemical, or thermal oxide films.[197,283,618,619] To accomplish this, one must be very careful about using the lowest possible pressure during the high temperature anneals, as interfacial SiC formation and/or surface roughening may otherwise occur. An interesting modification of this approach was demonstrated recently by Wilk *et al.*[283] They showed that the temperature of SiO desorption can be lowered by supplying a flux of Si atoms during the *in situ* preclean. Their process also resulted in a smoother surface, as can be seen from the STM images in Fig. 99.

3. The transition regime

For both the active and passive oxidation regions the surface remains relatively smooth. However, this is not the case if oxidation is performed in the transition regime, or during active oxidation at low temperatures, as was shown in Fig. 87. SEM experiments showed microscopic growth features, interpreted as Si islands as large as microns in size, covered by a thin oxide layer.[582] Ross and coworkers[268] used the term ''roughening regime'' to describe this unusual oxidation behavior, ascribed to surface roughening with a characteristic lateral scale of about 5.0 nm. Significant surface roughening in the transition regime was independently found by STM for Si(111)[289,301] and Si(100),[281] Fig. 100. Experiments by Sutherland *et al.*[234] showed the existence of a roughening regime during the initial oxidation of Si(111) with N_2O, but at much higher pressures than are observed for O_2 roughening.

The origin of surface roughening is not fully understood, and the shape of the transition regime in pressure-temperature space is only partially documented. Ross and coworkers[268] found a relatively narrow transition regime, whereas recent STM experiments[281,289,587] suggest that this regime covers several orders of magnitude in pressure.

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

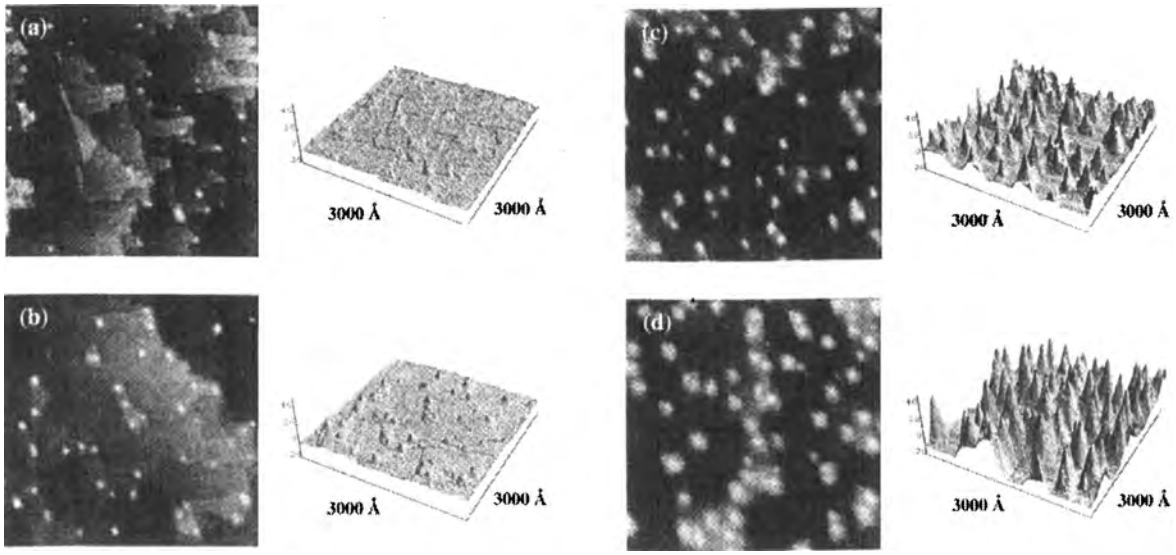


FIG. 100. Top and three-dimensional views of 300×300 nm^2 scanning tunneling microscopy images after Si(100) exposure to O_2 in the roughening regime (600 °C, 6×10^{-8} Torr) as a function of exposure: (a) 100 L, (b) 200 L, (c) 400 L, and (d) 800 L. 1 L=1 langmuir=10^{-6} Torr s [from Seiple *et al.* (Ref. 281)].

Roughening is thought to be caused by competition between the two simultaneous processes of oxide growth, and surface etching from the areas not covered by oxide islands.[268,301,591] However, neither HRTEM nor STM can probe the surface O directly, especially when the surface is very rough. Feltz and coworkers[301] used AES to complement their STM results and showed that O is present on the surface. This observation was later supported by MEIS experiments,[591] in which both the Si and O backscattering peaks were measured, Fig. 101. MEIS provides clear evidence for the presence of surface O in the transition region of pressure-temperature space, and both Si and O peaks demonstrate surface roughening. From the MEIS experiments the vertical roughness was estimated to be as large as 2 to 3 nm.

These observations suggest that once the oxide islands form, they passivate the Si under the oxide and hinder etching of the steps near them, although the etching reaction still takes place in between the oxide islands, as shown in Fig. 87. This process results in the formation of three-dimensional conical islands with heights as large as 4.0 nm,[281] shown in Fig. 100. The O atoms, in the form of a surface oxide, are assumed to at least partially cover these islands, whereas areas in between the islands are assumed to be free of O.

Oxide island growth and etching in the transition regime is kinetically limited. Thus time plays an important role in the roughening behavior. Therefore surface morphology should be described in three-dimensional pressure-temperature-time phase space, rather than by the conventional pressure-temperature phase diagram.[620–622] Seiple and Peltz showed that the roughness is not simply a function of O exposure, but depends on O_2 pressure or, equivalently, time, at a constant exposure.[289,587] It should also be mentioned that observed discrepancies in growth modes in the passive oxidation regime may be related to how close the oxidation parameters in such studies were to the transition regime.

B. Growth mechanisms of ultrathin oxides, beyond the Deal–Grove model

While the seminal paper by Deal and Grove[483] brought our understanding of the mechanism of thermal oxidation of Si to a new level of sophistication, much still remains under debate, especially in the limit of thin (sub-10 nm) films.[28,29,31,199,585,623] The Deal–Grove (DG) model[483] treats Si oxidation as the reaction of Si and O at the planar Si/SiO_2 interface, accomplished by O_2 transport to the interface of the growing film. The model is schematically depicted in Fig. 102. For thick films, the model predicts a parabolic dependence of oxidation time on oxide thickness because the growth is limited by diffusion. Further, in the limit of thin

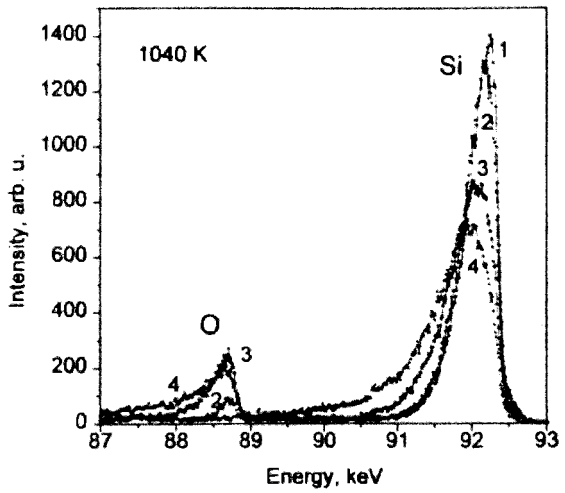


FIG. 101. Medium energy ion scattering spectra showing the development of the Si and O peaks in the oxidation transition region. Both the Si and O peaks show a low energy tail, characteristic of surface roughness. The oxidation conditions are: (1) clean Si, (2) 1040 K, 10^{-6} Torr, 3 min, (3) 1040 K, 10^{-6} Torr, 10 min, and (4) 1040 K, 10^{-6} Torr, 120 min [from Lu *et al.* (Ref. 591)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

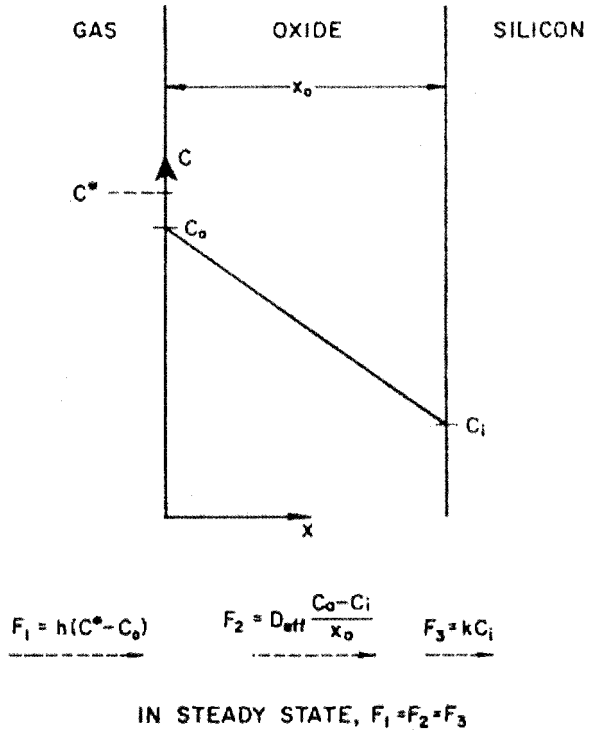


FIG. 102. Schematic illustration of the Deal–Grove model. The figure shows one-dimensional O concentration distribution (C), and O fluxes, F_1, F_2, and F_3, in the growing SiO_2 film [from Deal and Grove (Ref. 483)].

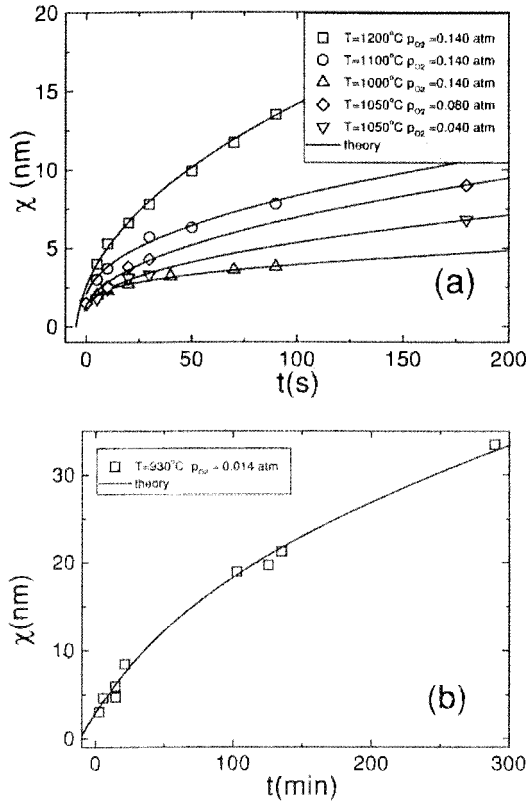


FIG. 103. SiO_2 growth kinetics data from various sources, compared with theory (solid lines) [from de Almeida *et al.* (Ref. 624)].

films, DG shows that the reaction rate at the interface governs the growth and results in a linear relationship between the thickness and the oxidation time for a given pressure and temperature, although the microscopic mechanism of the reaction which determines the rate constant is still unclear.

The original assumption of the DG model was that the reaction was first order between O and Si species. This approximation is not entirely appropriate in the solid state where the reaction takes place at the dense, lattice mismatched, and defect rich (suboxides, vacancies, interstitials, etc.) Si/SiO_2 interface. Another assumption of the model that becomes questionable in the thin film regime is the steady state assumption, in which all fluxes are assumed constant, and defined by the incoming flux of O_2 from the gas phase. Recently, it has been demonstrated[624] that without the steady state assumption it becomes possible to describe Si oxidation kinetic data very adequately, including the very initial regime, as is seen in Fig. 103.

The DG model yields oxide thickness as a function of the processing parameters temperature, oxidant pressure, and time. This kinetic approach works well for the parabolic growth stage. In the ''reaction-limited'' region, it is not clear that the linear dependence can be applied to the zero-thickness limit. Ellipsometric,[29,625] Fig. 104, as well as other studies, showed that there is a region of ''faster'' initial growth. These observations were the basis of several phenomenological models based on the DG formalism. A review of these models can be found elsewhere.[493] In one model,[73] for example, two exponential terms were added to account for the faster growth. In another model, reactive sites in the near-interfacial oxide, whose concentration exponentially decays with time, were introduced to account for the faster initial growth.[626]

The breakdown of the DG model in the important ultrathin regime motivated intense experimental and theoretical work aimed at elucidating diffusion and reactions on the atomic scale. Much recent progress in the experimental arena came from the use of powerful isotopic labeling methods, using both O and Si, starting from pioneering work by Rigo and his group.[210–214] A comprehensive review of isotopic methods applied to Si systems has recently been published.[25] Many studies involved the use of sequential oxidation of Si in $^{16}O_2$ and $^{18}O_2$, or in isotopically labeled H_2O, with subsequent analysis of the isotopes and their depth profiles by

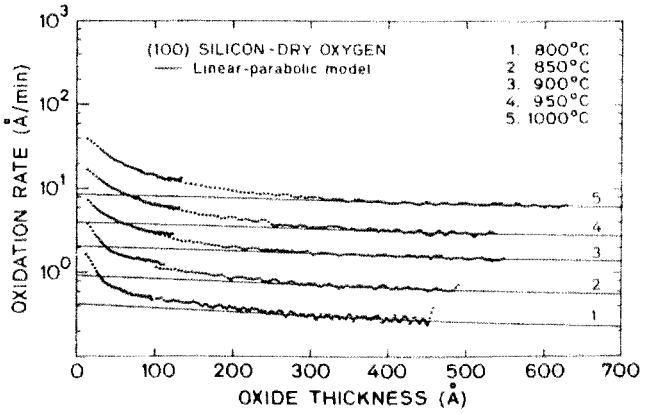


FIG. 104. Oxidation rate of Si(100) in dry O_2, measured by ellipsometry. A fast initial oxidation regime is observed [from Massoud *et al.* (Ref. 625)].

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

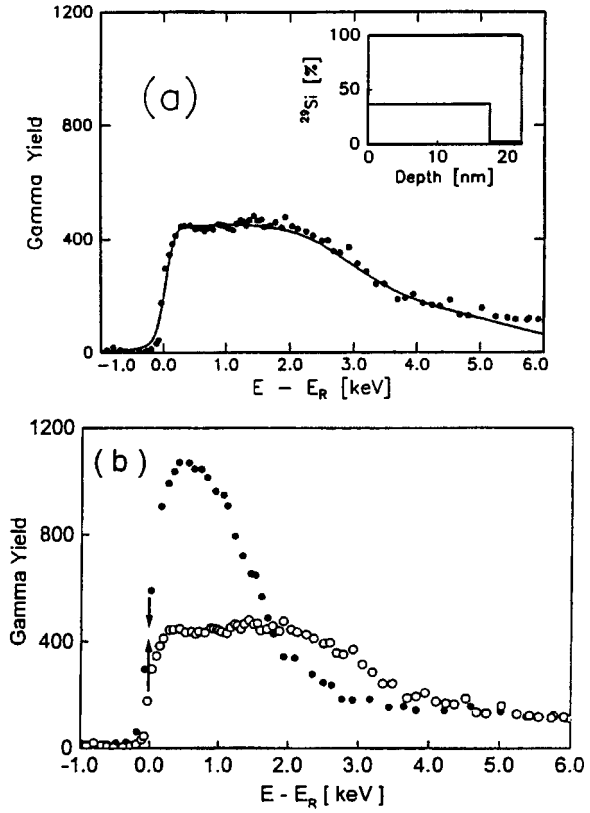


FIG. 105. Oxidation of an isotopically enriched (^{29}Si epitaxial layer) Si surface. (a) ^{29}Si nuclear reaction analysis excitation curve (solid circles) and simulated results (solid line) for an oxidized sample, with the ^{29}Si profile shown in the inset, and (b) ^{29}Si excitation curves of the initial ^{29}Si episample (solid circles) and after oxidation in O_2 [empty circles, same data as solid circles in (a)]. The arrows show the energy position of surface ^{29}Si atoms. One can see that the ^{29}Si stays at the surface after oxidation [from Baumvol *et al.* (Ref. 223)].

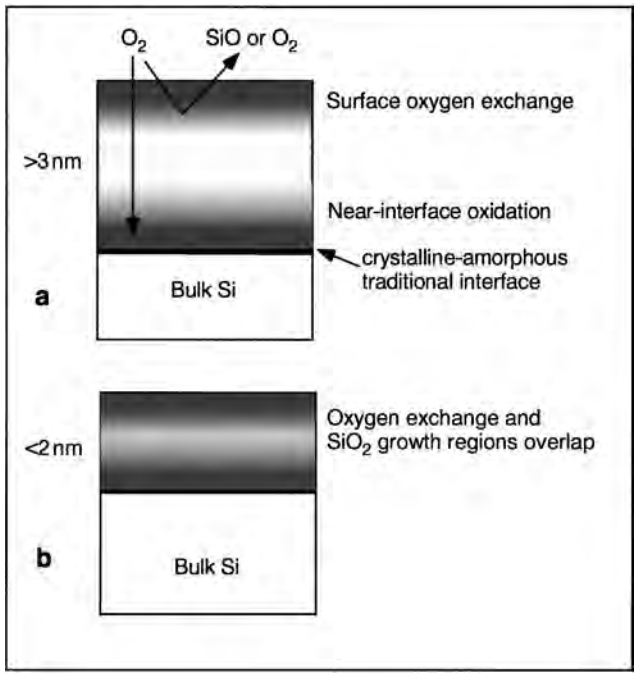


FIG. 106. Schematic model of the different regions where oxidation reactions occur: interface reaction (traditional Deal–Grove), near-interface reaction, and surface exchange reaction. In thicker (>3 nm) films, the regions are spatially separated, but in thinner films (<2 nm) they overlap [from Gusev *et al.* (Ref. 199)].

NRA[210–214,216,627–629] (see, for example, Fig. 33), MEIS,[199,200,202,204,238,630,631] (see, for example, Fig. 94), and SIMS.[228,232,247] In a related study, a layer of deposited ^{29}Si was used to trace the movement of Si during oxidation,[223] as is shown in Fig. 105. On the theoretical front, state-of-the-art *ab initio* calculations have shed further light on the complex structures and reactions during Si oxidation.[598,632–640]

The new features experimentally observed in the ultrathin regime can be summarized as follows.[199,202] In addition to the expected DG oxidation at the interface, two other reactions occur: an O exchange reaction near the oxide surface and an oxide growth reaction near the interface. These reactions are schematically depicted in Fig. 106. The latter reaction presumably occurs throughout a transition region between crystalline Si and stoichiometric, amorphous SiO_2. The transition region at the interface seems to play an important role in the oxidation process. Based on the ^{29}Si labeling experiment,[223] it was concluded that Si atoms from the substrate do not diffuse through the growing oxide.

An important observation of the MEIS work[199,202,204,631] is that the growth reaction takes place not at a sharp interface, but throughout the transition region between Si and stoichiometric SiO_2; see Fig. 106. The implication of this result is twofold: (i) any theoretical model of Si oxidation must consider that oxidation is not just a first order chemical reaction at a sharp interface, and (ii) more studies are needed to understand the exact structure and composition of the transition region. One needs to know how the transition region is affected by the oxidation process, as well as how the properties of the transition region are correlated with electrical defects, many of which are known[28,29,31,122,124,129] to be localized at the interface and near-interface regions.

Several models include the near-interfacial region as an element of the oxidation process. For example, Tiller[641] and subsequently others[642–646] suggested that Si interstitials formed at the reaction interface diffuse, or are injected into the near-interfacial oxide, where they may subsequently react with the O diffusing towards the interface. Si injection was directly observed by STM during the very initial stages of O interaction with Si(100),[647] as is shown in Fig. 107. A similar scenario, but with SiO formation at the interface and diffusion towards the surface, has been suggested by others.[598,639,648,649] Some researchers postulate Si fragments, or clusters, in the oxide[72,214] and their subsequent reoxidation. Another reactive layer model[495,585] further considers a thin reactive SiO layer near the interface. However, according to this model, the reaction takes place on top of, and not throughout, the reactive layer, inconsistent with MEIS results.[199,200,630] One can propose a more general model[199,200,630] in which the near-interfacial reaction is caused by O interaction with incompletely oxidized Si, i.e., suboxides, Si interstitials, clusters, and/or SiO. Again, we stress that the near-interface reactions become most important for ultrathin films. For thicker oxides, the near-interfacial reactions still probably occur; however, since the reaction region in this case is much thinner than the thick-

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

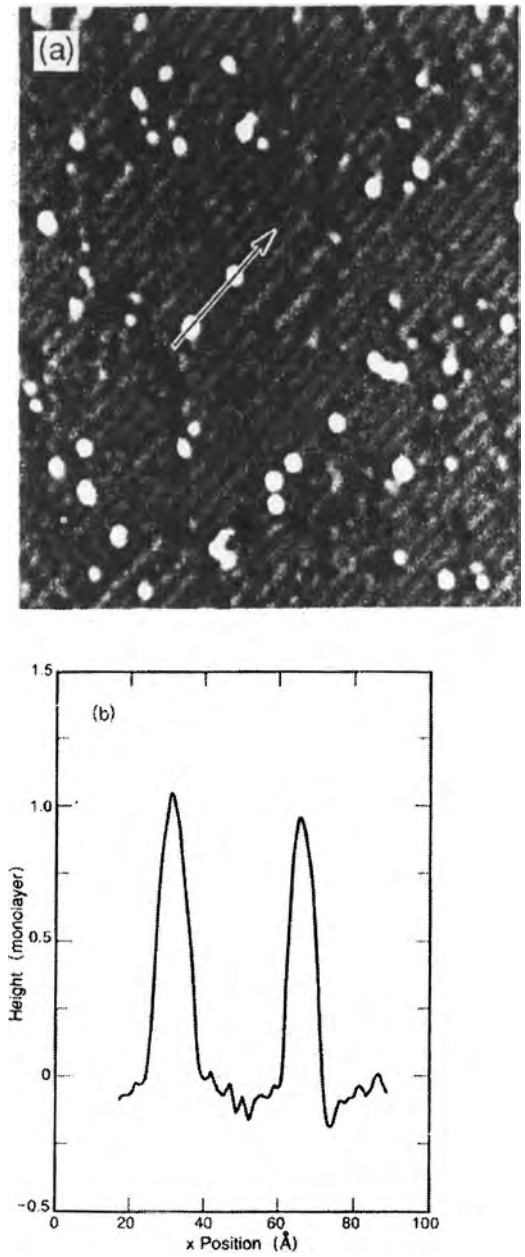


FIG. 107. A scanning tunneling microscopy image of the Si(100) surface exposed to O_2 at room temperature. The O_2 exposure produced protrusions, seen as white spots. The bottom picture shows a line scan through the protrusions. One monolayer of Si(100) is 0.14 nm high [from Cahill *et al.* (Ref. 647)].

ness of the film, they may, at least geometrically and possibly even kinetically, be considered as one reaction at the interface, akin to the DG model.

The surface exchange reaction is perhaps even more complicated than the interface growth reaction.[199,200,211–214,224,629,630] The mechanisms of O uptake, reaction, and loss from the growing oxide film are not well understood. One group claimed that the reaction was related to an exchange of atomic O with the SiO_2 network.[212] This is consistent with the provocative suggestion that O, and not O_2, is the primary diffusing species in SiO_2.[637,650] Others tried to correlate the O exchange with H_2O traces present during oxidation.[651] It has also been claimed that surface defects, e.g., peroxy-bridged O, may be involved in the surface reaction. Despite the fact that the surface exchange reaction does not directly contribute to the growth of the SiO_2 layer, it may be important for sub-2.0 nm films, where both surface exchange and near interface reactions overlap in space, Fig. 106, and may therefore influence each other. A recent study shows that an O exchange mechanism is also operative at the Si/SiO_2 interface.[652]

Pasquarello *et al.*[633] performed first principles molecular dynamics calculations, in which electronic structure evolves self-consistently with atomic motions, to explore structural rearrangements at the interface between crystalline Si and disordered SiO_2 during high temperature oxidation. The calculations revealed interesting features. The upper layer of the Si substrate contained about a quarter of a monolayer of extra Si atoms, and they formed intralayer Si–Si bonds. It was also found that changes in the bonding network near the interface occur via transient exchange events in which O atoms are momentarily bonded to three Si atoms. This metastable configuration enables the interface to evolve without leaving dangling bonds. Based on these calculations, the following mechanism for the near-interfacial reaction was proposed.[633] Incoming O atoms react with Si–Si bonds in a reaction layer approximately 0.5–1.0 nm thick, near the interface. At high reaction temperatures, network rearrangement, via the formation of metastable threefold coordinated O atoms within the reaction layer, leads to a constant exchange motion of O atoms through to the interface. This process disturbs the Si lattice, which in turn promotes the incorporation of O into the disturbed network, resulting in the formation of new interfacial oxide. This mechanism drives some excess Si atoms into the Si and SiO_2 layers adjacent to the interface. The new Si–Si bond ''injected'' into the reaction layer reacts again with incoming O as the oxidation reaction proceeds. This scheme, based on network motion in the reaction layer, is consistent with isotopic labeling MEIS experiments,[202] such as are illustrated in Fig. 108, which show evidence for motion of O atoms near the interface and provide further evidence and a visualization of the excess Si near the interface.

The formation of the threefold coordinated O atoms was also deduced from density functional theoretical calculations.[634,635] Using first principles, total energy calculations it was shown that the key process in the atomic scale reactions during the formation of thin thermal SiO_2 films on Si, as well as SiO_2 precipitation in O-rich Si crystals, is the emission of Si interstitials. This process helps to eliminate dangling bonds and therefore explains the low concentration of defects at the Si/SiO_2 interface.

The structural and electronic properties of the (100) Si/SiO_2 interface and O diffusion in amorphous SiO_2 were studied using first principle calculations by Ng and Vanderbilt.[636] The calculations showed an O deficient, i.e., Si suboxide, transition region at the interface, Fig. 109, of thickness ~2.0 nm. Calculations of the oxidation kinetics in SiO_2 suggested that the peroxyl linkage configuration may be responsible for O diffusion in the growing silica film, as is suggested by Fig. 110. This mechanism is similar to Ha-

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

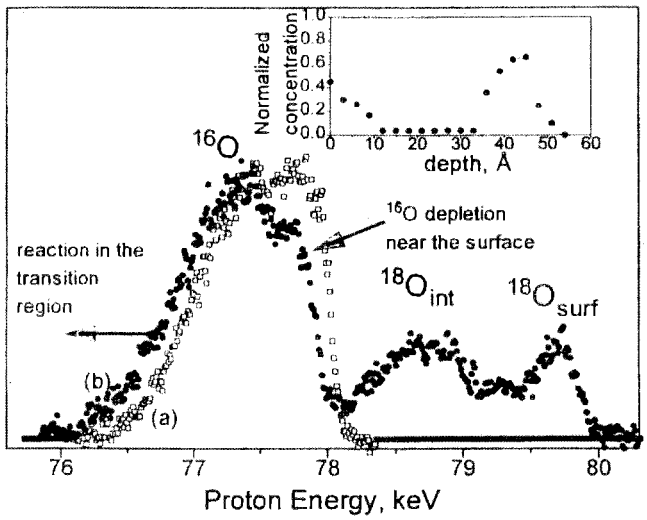


FIG. 108. Oxygen medium energy ion scattering spectra before (solid symbols) and after (open symbols) reoxidation of an initial 4.5 nm Si $^{16}O_2$/Si film in $^{18}O_2$. ^{18}O incorporation at/near the interface and at the outer oxide surface is observed (see also Fig. 31). The loss of ^{16}O at the surface is seen. The ^{16}O peaks become broader on the lower proton energy side after the reoxidation, indicative of isotopic mixing at the interface [from Gusev *et al.* (Ref. 202)].

mann's peroxy-linkage diffusion model[637] deduced from density functional calculations.

Unfortunately, still unresolved is a fundamental and quantitative understanding of (i) the O interaction with Si either at the clean surface or the Si/SiO_2 interface, (ii) what fraction of the oxidation takes place at the ''formal'' interface as compared to the near interfacial region, and (iii) what is the steady state concentration of Si–Si bonds, describable, for example, as suboxides and interstitials, as a function of distance from the interface. This level of information is needed if one attempts a more accurate, atomic scale revision of the DG model.

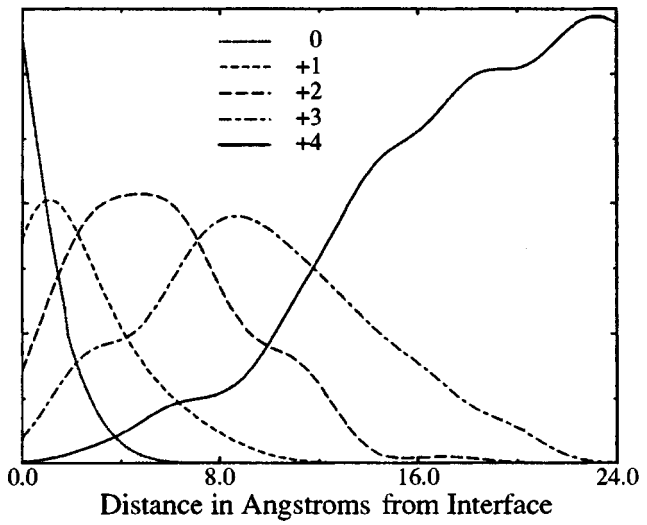


FIG. 109. Distribution of the Si oxidation states (Si^{1+}, Si^{2+}, Si^{3+}, and Si^{4+}) as a function of distance from the interface, calculated from Monte-Carlo simulations [from Ng and Vanderbilt (Ref. 636)].

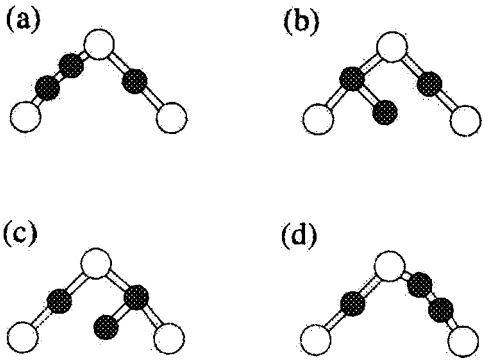


FIG. 110. Proposed mechanism for diffusion of atomic O in amorphous SiO_2, via peroxyl bonds. The black atoms are O [from Ng and Vanderbilt (Ref. 636)].

VI. THE Si/SiO_xN_y SYSTEM

Ultrathin Si–O–N layers, with essentially the same dielectric constant as SiO_2 due to their low N concentration, may replace SiO_2 for thicknesses $\leqslant 2$ nm, since the N offers process latitude and protection against B and other impurity penetration through the gate dielectric. Oxynitrides may also enhance reliability and reduce hot electron induced degradation. Several excellent reviews of Si–O–N layers have been written.[2,37,38]

A. Oxynitride properties

1. Thermodynamics of the Si–O–N system

The bulk phase diagram of the Si–O–N system[653] is shown in Fig. 111. The diagram consists of four phases: Si, SiO_2, Si_3N_4, and Si_2N_2O. The three compound phases are composed of similar structures comprising SiO_4, SiN_4, and SiN_3O tetrahedrals, implying that SiO_2 can be converted to Si_2N_2O and finally to Si_3N_4 by replacing O with N in a 2N/3O ratio. However, the Si_3N_4 and SiO_2 phases never coexist in the bulk under equilibrium conditions. Si_2N_2O is the only thermodynamically stable form of Si–O–N.[653–657]

At chemical equilibrium, N should not incorporate into an SiO_2 film as long as almost any partial pressure of O, i.e., $>10^{-20}$ atm, is present, as is implied in Fig. 111. A puzzling question is why N atoms are incorporated at all in SiO_2 as a result of the thermal decomposition of N_2O[173,226,243,658–660] or NO,[158,169,201,203,661,662] since the partial pressures of oxidizing species, which are decomposition by-products, are very large. At least two reasons for the presence of N in the SiO_2 film can be suggested. First, N atoms may simply be kinetically trapped at the reaction zone near the interface, and thus the N is present in a nonequilibrium state. In this model it is assumed that the N is incorporated into the film during oxynitridation and reacts only with Si–Si bonds at or near the interface, not with Si–O bonds in the bulk of the SiO_2 overlayer. Alternatively, the N at the interface may indeed be thermodynamically stable, due to the presence of free energy terms not represented in the bulk phase diagram. For example, N may lower the interfacial strain, known to exist at the Si/SiO_2 interface.[226,663–665] This could explain why incorporated N, especially in N_2O or NO Si–O–N films, is often associated with the Si/SiO_2

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

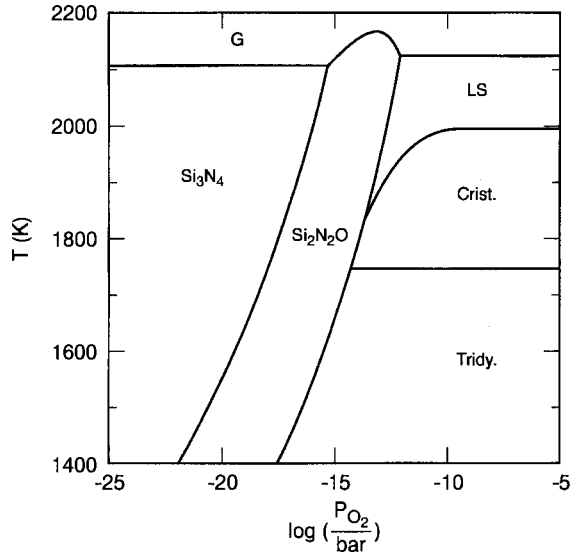


FIG. 111. Thermodynamic (bulk) phase diagram of the Si–O–N system [from Hillert *et al.* (Ref. 653)].

interface.[135,173,201,243,260] Even when N is implanted into Si it tends to incorporate into SiO_2 and migrate to the Si/SiO_2 interface after subsequent oxidation.[519,666] Therefore there is some evidence to suspect that the N plays a specific role at the interface, but also that it is not stable away from it, in the SiO_2 bulk.[233,667]

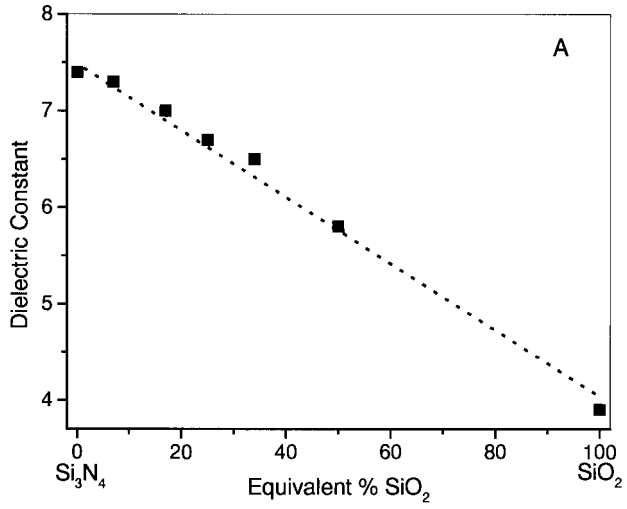
2. Physical properties

Figure 112 shows the change in dielectric constant and band gap of Si–O–N films as a function of N content. In this case, the dielectric constant (κ) was assumed to increase linearly with increasing fraction of Si_3N_4, from $\kappa(SiO_2)=3.9$ to $\kappa(Si_3N_4)=7.5$.[111] A very recent study shows a departure from linearity;[668] κ is found to be higher than the predicted values.

Due to the higher κ of Si_3N_4, an Si–O–N film having the same capacitance as an SiO_2 film will be physically thicker. However, at the same time the band gap, and therefore the barrier height for electron and hole tunneling, decreases with increasing N content. In addition, there is a possible change of the effective mass of the carriers. All of these factors must be taken into account in understanding the tunneling properties of ultrathin Si–O–N films. Finally, the refractive index (at 635 nm) also increases with the amount of incorporated N from $\eta(SiO_2)=1.46$ to $\eta(Si_3N_4)=2.0$, as is shown in Fig. 12.

3. Diffusion barrier properties of oxynitride layers

Boron penetration through the gate dielectric causes threshold voltage shifts and degrades reliability.[669–673] An important property of Si–O–N layers is their ability to act as a diffusion barrier to impurities, notably B.[674–681] Oxygen, N_2O, and NO diffusion rates are also lowered in Si–O–N films, significantly retarding the rate of further oxidation or nitridation, as can be seen, for example, in Fig. 113. One explanation for the enhanced diffusion resistance is that the density of Si_3N_4 and Si–O–N is higher than SiO_2 (ρ_{SiO_2} $=2.3\,g/cm^3$ and $\rho_{SiN}=3.1\,g/cm^3$). Therefore the diffusivity of N_2O, NO, O_2, N_2, as well as other nonreactive molecular species such as the noble gases should be lower in the N containing films. Studies of B penetration in SiO_2 films of slightly varying density have shown enhanced diffusion resistance to B with excess film density.[682] However, the rigidity of the N bonded lattice might be the basis of an equally important explanation. The three bonds connected to each N atom, such as in Si_3N_4, are more constrained than the two bonds connected to each O atom in SiO_2. Whereas the Si–O–Si bond angles can vary from 120° to 180° with little change in energy, the Si_3N_4 lattice is much more constrained. This may contribute to a decrease in the ability of the nitrided lattice to permit diffusion of atoms and small molecules.



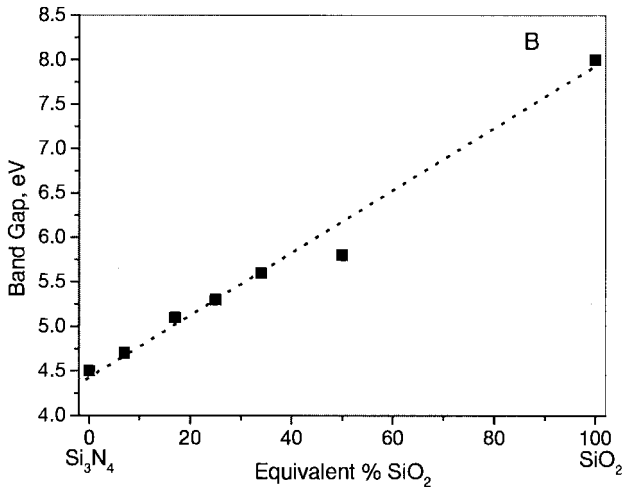


FIG. 112. Dielectric constant (a) and band gap (b) as a function of N content in the Si–O–N system [from Brown *et al.* (Ref. 111)].

To explain the ''stopping power'' of the N in Si–O–N films, a model assuming B diffusion via peroxy linkage defects (Si–O–O–Si bonds), whose concentration changes under different processing conditions and film thicknesses, has been suggested.[683] For a 1.5 nm SiO_2 film, the diffusivity at

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

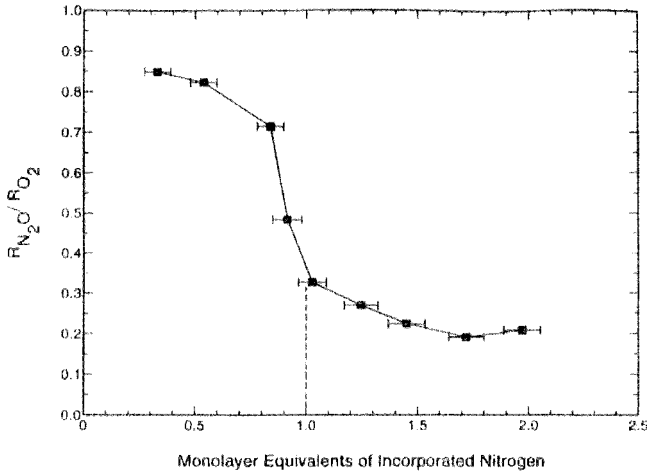


FIG. 113. The ratio of N_2O-oxide to O_2-oxide growth rates (for ~10 nm films) as a function of final N content of the N_2O oxides [from Green *et al.* (Ref. 521)].

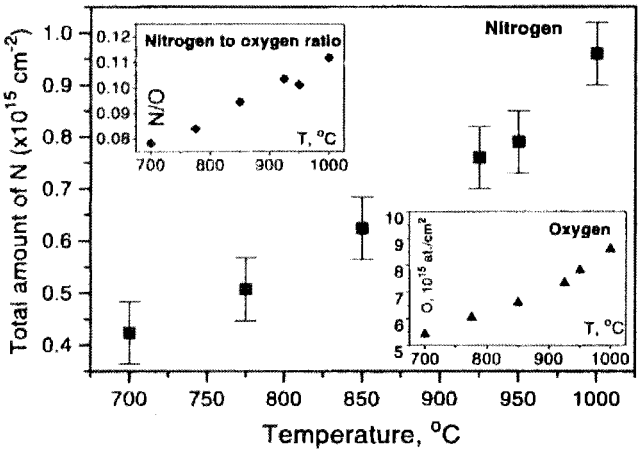


FIG. 114. Concentration of N as well as O (right inset) and N/O ratio (left inset) in ultrathin SiO_2 films annealed in NO, as measured by medium energy ion scattering [from Gusev *et al.* (Ref. 203)].

900 °C would increase by a factor of 24 as compared with 10 nm oxides. According to this model, the role of N is to compete with B for occupation of the defect sites. Another model, in which B diffuses substitutionally for Si atoms, has also been suggested.[678] The role of the Si–N bond is to impede substitution for that Si atom. The model incorporated a Monte Carlo simulation and showed good agreement with experimental data. Several groups have also suggested that a dative B–N bond may be formed, thus hindering the diffusion of B in the dielectric.

Another interesting aspect of the diffusion barrier properties of Si–O–N films is that Si interstitials generated at the interface during oxynitridation are blocked from diffusing into the oxide. This results in an enhanced flux of the interstitials into the Si substrate, which in turn yields an increased density of oxidation induced stacking faults. These may then influence the extent of oxidation induced transient diffusion.[684,685]

B. Oxynitridation processes

Nitrogen may be incorporated into SiO_2 using either thermal oxynitridation or annealing, or chemical and physical deposition methods, as is shown in Table VI. Thermal nitridation of SiO_2 in NO or N_2O generally results in a relatively low concentration of N in the films, on the order of 5×10^{14} N/cm^2, the equivalent of <1 monolayer of N in the thin SiO_2 film. Whether annealing preoxides, or oxynitriding the Si surface directly, the N content increases with temperature.[173,203] To attain higher N concentrations, other methods such as CVD,[686] JVD,[513] ALD,[687] or nitridation by energetic N particles can be used.[525,688] These nitridation methods can be performed at lower temperatures, ~300–400 °C. However, the deposition methods are nonequilibrium and subsequent thermal processing steps are often required to improve film quality through minimization of defects. Because the thermodynamics of the Si–O–N system and the kinetics of N incorporation are rather complex, these different methods produce Si–O–N films with different total N concentrations and depth distributions.

1. NO processing

Oxynitridation of Si, or annealing of SiO_2, in nitrous (N_2O)[689,690] or nitric (NO)[662,691] oxide is the most popular processing method for making Si–O–N films by conventional thermal routes. NO is believed to be responsible for N incorporation in both cases.[2,158,233,662,667,692] If NO is the species responsible for N incorporation, oxynitridation in pure NO should be considered for ultrathin dielectrics, since it results in nearly self-limiting growth behavior.[157] From the practical viewpoint, the slower growth of Si–O–N relative to pure SiO_2 facilitates good thickness control in the ultrathin regime during high temperature processing. Compared to N_2O, oxynitridation in NO results in more N incorporation at a given temperature.[169,170,201] In addition, NO Si–O–N films exhibit lower leakage currents and interface defect densities, as well as improved electrical stress properties.[157,170,662,691,693] However, excessive N concentration at the interface may lead to mobility degradation.[694]

Figure 114 shows the total amount of O and N in NO-annealed ultrathin SiO_2 films on Si(100), after 1 h anneals in the temperature range 700–1000 °C.[203] As the temperature increases, the total amounts of both N and O increase, as well as the ratio of N to O in the film. It is believed that NO diffuses to the interface and dissociates there, thereby oxidizing and nitridizing the Si.[692] Quantitative MEIS N depth profiles[203] of these Si–O–N films are shown in Fig. 115, in which it can be seen that the width of the N-containing region increases with temperature. As the position of the interface, deduced from the O depth profile and marked by arrows, propagates deeper into the Si substrate with increasing temperature, the N follows its movement. In all cases, the N is distributed almost evenly in the films except for the very near-surface SiO_2 region. These results are inconsistent with a model of a continuous Si_3N_4 layer near the interface. However, multiple features in angularly dependent core level (N 1*s* and Si 2*p*) photoemission spectra,[137,169,201] and the multiphase nature of electronic paramagnetic resonance (EPR) signals from Si–O–N films,[695] suggest more complex local chemical bonding in the film.

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

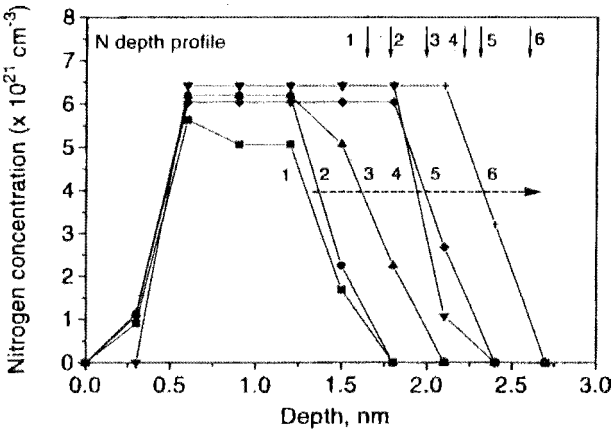


FIG. 115. Nitrogen medium energy ion scattering depth profiles, as a function of the distance from the outer surface, for SiO_2 films annealed in NO at (1) 700 °C, (2) 775 °C, (3) 850 °C, (4) 925 °C, (5) 950 °C, and (6) 1000 °C. The arrows show the interface position for each film [from Gusev *et al.* (Ref. 203)].

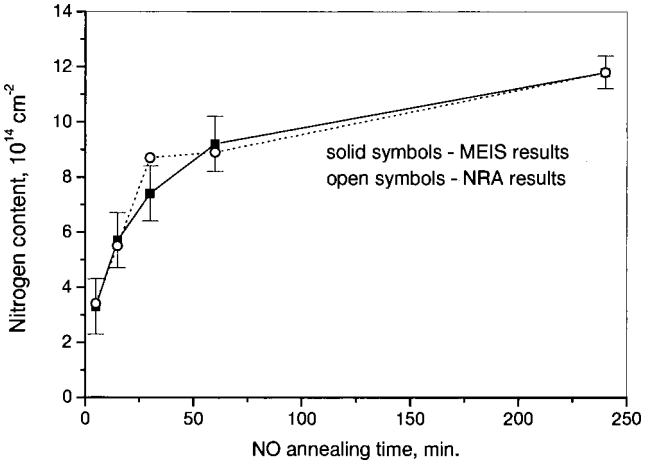


FIG. 116. Kinetics of N incorporation into a 4.5 nm SiO_2 preoxide annealed in NO at 850 °C. The solid symbols represent the data obtained by medium energy ion scattering; empty symbols show nuclear reaction analysis results [E. P. Gusev and M. L. Green (unpublished work)].

Due to the relatively high concentration of N incorporated into NO films, the kinetics of reoxynitridation are very slow. To make a thicker NO film, an SiO_2 preoxide of desired thickness can first be grown, followed by an NO anneal. Typically NO annealed preoxides yield N distributions different from the NO grown films, in that the N becomes concentrated near the interface. The N pileup near the interface results from NO molecular diffusion, and subsequent incorporation, at the interface. The kinetics of N incorporation in a 4.5 nm SiO_2 film annealed in NO at 850 °C are shown in Fig. 116. One can see that after a fast initial accumulation, the rate of N incorporation saturates. The total concentration of N for an NO-annealed preoxide is comparable with the concentration of an NO grown film oxidized under equivalent conditions, at least for long oxynitridation times. Also noteworthy from Fig. 116 is the excellent agreement between MEIS and NRA N data.

2. N_2O processing

Oxynitridation in N_2O is particularly attractive because it allows one to incorporate a small but significant amount of N near the Si–O–N/Si interface, typically $\sim 5 \times 10^{14}$ N/cm^2, and because of its processing similarity to O_2. However, among other factors, oxynitridation in N_2O is complicated by the fast gas phase decomposition of the molecule into N_2, O_2, NO, and O at typical oxidation temperatures, 800–1100 °C.

a. Gas phase N_2O decomposition at high temperatures. In contrast to NO, a relatively stable molecule, N_2O rapidly decomposes at high temperatures. The decomposition is a complex process. Gas flow rate, temperature, partial pressure of N_2O, reactor type (e.g., rapid thermal processing versus furnace) and geometry, and gas phase impurity levels all affect the kinetics and final distribution of products.[696,697] An additional complication is that N_2O decomposition is strongly exothermic and can cause temperature and therefore film thickness nonuniformities across the reactor.[698]

NO_x chemistry has been studied extensively for many years by environmental scientists. Of the many possible NO_x reactions known to occur, Table VII, the first five key steps seem to dominate the N_2O decomposition to NO.[699] The rate limiting reaction is the first step

$$N_2O \rightarrow N_2 + O. \tag{13}$$

This decomposition obeys first order kinetics, and thus the initial rate law for N_2O decomposition is

$$R_{\text{init}} = 2k_{1[N_2O]}, \tag{14}$$

which rapidly changes to

$$R_{\text{late}} = k_{1[N_2O]} \tag{15}$$

as the reaction proceeds, where k_1 is the reaction constant of the initial reaction. The apparent activation energy for the decomposition of N_2O is 2.5 eV/molecule. The characteristic decay time of the N_2O concentration is on the order of ~ 20

TABLE VII. Reaction scheme for N_2O decomposition [from Gupta *et al.* (Ref. 699)].

1. $N_2O \rightarrow N_2 + O$
2. $N_2O + O \rightarrow NO + NO$
3. $N_2O + O \rightarrow N_2 + O_2$
4. $O + O \rightarrow O_2$
5. $NO + O \rightarrow NO_2$
6. $NO_2 + O \rightarrow NO + O_2$
7. $NO_2 + NO_2 \rightarrow NO + NO + O_2$
8. $NO_2 \rightarrow NO + O$
9. $NO_2 + NO_2 \rightarrow NO_3 + NO$
10. $NO_3 + NO \rightarrow NO_2 + NO_2$
11. $NO_2 + O \rightarrow NO_3$
12. $NO_3 \rightarrow NO + O_2$
13. $NO_3 + O \rightarrow O_2 + NO_2$
14. $NO_2 + NO_2 \rightarrow N_2O_4$
15. $N_2O_4 \rightarrow NO_2 + NO_2$
16. $NO_2 + NO_3 \rightarrow N_2O_5$
17. $N_2O_5 \rightarrow NO_2 + NO_3$
18. $O_2 + O \rightarrow O_3$
19. $O_3 \rightarrow O_2 + O$
20. $O_3 + O \rightarrow O_2 + O_2$
21. $O_3 + NO \rightarrow NO_2 + O_2$

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

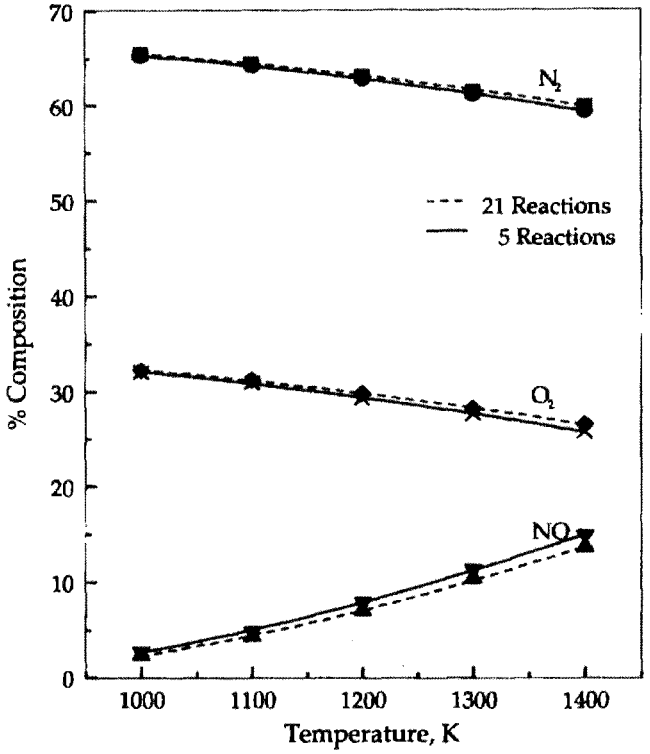


FIG. 117. Equilibrium concentrations of the major by-products (N_2, O_2, and NO) of the gas phase decomposition of N_2O calculated using the scheme shown in Table VII [from Gupta *et al.* (Ref. 699)].

s at 1000 K and decreases with increasing temperature. Oxygen atoms then react further by the following two key reactions:

$$N_2O+O\rightarrow 2NO, \tag{16}$$

$$N_2O+O\rightarrow N_2+O_2. \tag{17}$$

The branching ratio for these two reactions lies between 0.1 and 0.5 and varies with the specific conditions. The rate law for NO formation is given by Eq. (15), and the apparent activation energy for the formation of NO is 2.4 eV/molecule.

The main products of N_2O decomposition are N_2, O_2, and NO, and the equilibrium concentration of NO increases with temperature,[699] as is shown in Fig. 117. Since N_2 is much less reactive than O_2 and NO, one might expect that a properly chosen mixture of NO and O_2 would produce a Si–O–N film similar to that grown in N_2O, but this is not the case. Oxynitridation in various mixtures of NO and O_2 is more similar to NO oxynitridation than to N_2O oxynitridation.[700] This suggests that there are other active species present during N_2O decomposition which are important in the nitridation process. Atomic O is believed to play a key role in N_2O oxynitridation.[237,667,696] Though the equilibrium concentration of atomic O is rather low, the transient concentration of atomic O created in the first step of the decomposition process may be relatively high, especially if N_2O decomposition takes place near the wafer. Since O radicals are very reactive, even a small partial pressure of O may have a significant effect on oxynitridation.

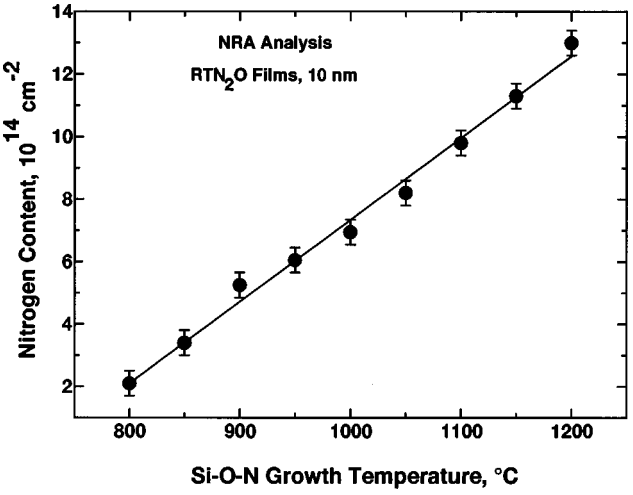


FIG. 118. Nitrogen content of 10 nm Si–O–N films grown in N_2O by rapid thermal oxidation at 1000 °C as measured by nuclear reaction analysis [from Green *et al.* (Ref. 173)].

b. N incorporation and removal during N_2O oxynitridation. Under equivalent conditions, N_2O results in less N incorporation than NO.[201] The total concentration of N increases with film thickness[701] as well as with N_2O oxynitridation temperature,[173] as can be seen from Fig. 118. This implies that N_2O oxynitridation may not be an efficient N incorporation mechanism for films thinner than ~3 nm. The N distribution in the films is sensitive not only to the processing conditions, but also to the reactor type.[662,667,696] Rapid thermal (RT) N_2O films show N pileup near the interface, while the distribution of N in the furnace-grown films is broader.[201] In the RTN_2O case the decomposition takes place near the hot wafer, and most of the decomposition products, including atomic O, can diffuse to the wafer. In a conventional furnace N_2O may decompose in the hot inlet of the furnace before it reaches the wafer. This depletion effect also explains the observation that the slower the input flow, the lower the N incorporation rate.[658,696]

The fundamental difference between oxynitridation in N_2O and NO is that while both incorporate N via NO reactions near the interface, in the N_2O case the N incorporation occurs simultaneously with N removal from the upper layers of the film.[233] The final N concentration and distribution is influenced by a competition between N incorporation and removal. The removal reaction likely involves O.[667] Since the reactivities of NO, N_2O, and O_2 with Si, SiO_2, and Si–O–N are quite different, properly chosen sequences of thermal reactions with Si can lead to Si–O–N films with different N concentrations and profiles, and therefore electrical properties. Based on an understanding of the kinetics and thermodynamics of N incorporation in SiO_2, one can "engineer" the N profile in an ultrathin dielectric.[702] Nitrogen profile engineering has also been accomplished using an O and N radical deposition technique.[703]

3. Nitridation in NH_3

Nitridation in NH_3 was one of the first methods used to incorporate relatively high (~10–15 at. %) concentrations of

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

N into SiO_2 films.[704–706] Nitrogen piles up both at the interface and the outer surface during the initial stages of nitridation, unlike the case of N_2O nitridation, and the N containing region near the interface is about 3 nm wide. The concentration of N slowly increases with NH_3 nitridation time, and the N distribution becomes more uniform in the film.[707,708] The thickness of the film remains essentially unchanged during nitridation. Nitrogen incorporation is enhanced by decreasing the SiO_2 film thickness. NH_3, directly reacted with Si, has also been used to form thin Si_3N_4 layers, although they may contain substantial O if either the ambient or the NH_3 contain H_2O or O.[128,709–711]

Ammonia nitridation introduces high concentrations of H into SiO_2 films, which can act as electrical traps. SIMS analysis shows that the H concentration increases monotonically with nitridation time and temperature. The H tends to pileup near the interface.[712] It was shown that the high concentration of H can be reduced by a postnitridation anneal in a H-free ambient, e.g., N_2. It was also found that the rate of H removal is not dependent on the annealing gas, consistent with thermally activated out-diffusion of H from the film.[707,708] Based on the detrimental effects of H on device performance, lighter nitridation, i.e., at lower temperature for shorter times, is desirable since it introduces less H. Detailed isotopic studies of the behavior of H,[218] as well as O and N,[713] in NH_3-nitrided SiO_2 have been carried out.

Ammonia nitridation of SiO_2 for gate dielectric applications has generally fallen into disfavor due to the deleterious effects of the incorporated H. However, reasonable electrical results have been reported[714,715] and there are still applications for NH_3 nitridation in the growth of some stacked SiO_2/Si–O–N/SiO_2 gate[716] and tunnel dielectric layers.[717]

4. Nitridation in N_2

Although N_2 is relatively inert, annealing of SiO_2 films in N_2 results in an initial reduction of fixed oxide charge.[536] This behavior was attributed to the formation of an Si–O–N layer near the interface, as detected by XPS.[168] This work was performed in a furnace at high temperatures (>925 °C), for long times (≥1 h). To reduce the thermal budget, one can form Si–O–N in nominally pure N_2 by rapid thermal processing.[718] The term ''nominally'' means here that although the input N_2 gas stream is purified at the point of use, and is therefore extremely free of contaminants (typically less than 1 ppb each of H_2O, O_2, CO_2, and CO), a cold wall RTP module contributes impurities to the ambient through outgassing from the walls. N_2 reacts with Si at moderate temperatures (850–1050 °C) in an RTP module (due to the presence of gas phase impurities) to form films <1.2 nm thick, as measured by ellipsometry, cross-sectional TEM, and MEIS. Figure 119 illustrates N content (measured *ex situ* by NRA) as a function of N_2 nitridation time for RTN_2 treatment at various temperatures.[718] At 850 °C, the N content is almost constant with time, whereas at the higher temperatures it increases and then may saturate with time. It can be seen from Fig. 119 that anywhere from 0.2 to 3 monolayer equivalent of N can be incorporated, depending upon temperature and time. [A monolayer equivalent is the concentration of the species, as if it were condensed at a two-dimensional interface or surface, in units of monolayers (one monolayer on Si(100) is $6.8\times10^{14}\,cm^{-2}$).] Oxygen and N depth profiling by MEIS shows a fairly uniform distribution of the elements in the films. Other researchers have also seen the formation of Si–O–N layers during high temperature RTP.[719]

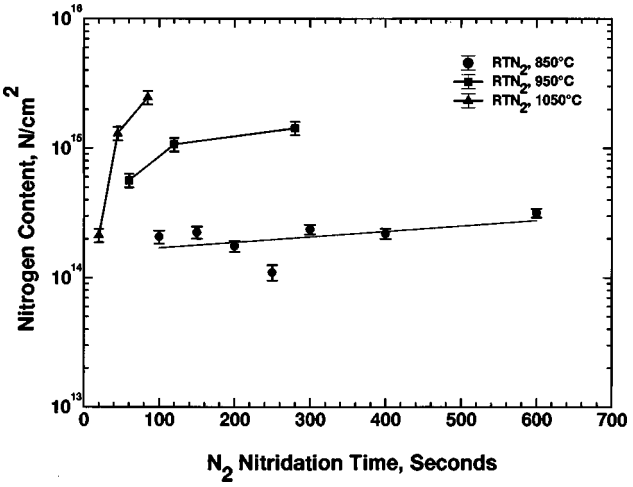


FIG. 119. Kinetics of N incorporation during rapid thermal processing in N_2 at 850 °C (circles), 950 °C (squares), and 1050 °C (triangles) [from Green *et al.* (Ref. 718)].

VII. THE POST-SiO_2 ERA: ALTERNATE GATE DIELECTRICS

SiO_2 gate dielectric thickness is continually decreasing with device scaling,[16] as is illustrated in Fig. 3. SiO_2 or lightly nitrided Si–O–N gate dielectrics are expected to be useful to thicknesses of about 1.3 nm.[17,45] Thinner films will exhibit excessive gate leakage current, Fig. 5, and diminished drive current, Fig. 7, thus requiring the implementation of alternate gate dielectrics. It will not be easy to replace SiO_2, since with the exception of its lower dielectric constant, it is an ideal material (Table I). Alternate gate dielectrics will introduce many complicated materials science and process integration issues, but many of these will be addressed first for back-end capacitor applications,[720–722] before the necessary introduction into the more demanding gate dielectric application, perhaps 5 years away.

TABLE VIII. Minimum essentials for high-κ gate dielectric technology.

Thermodynamic stability on Si with respect to formation of SiO_2 and MSi_x
Amorphous
$9\leqslant\kappa\leqslant25$
Lower leakage than SiO_2 at t_{ox}(eq)
Low D_{it} ($\leqslant5\times10^{10}\,eV^{-1}\,cm^{-2}$)
Deposition technique should be capable of interface control (prevention of adventitious SiO_2 growth)
Conformal growth
Many other considerations (etchability, diffusion resistance to oxygen, dopants and impurities, oxide defects, etc.)

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

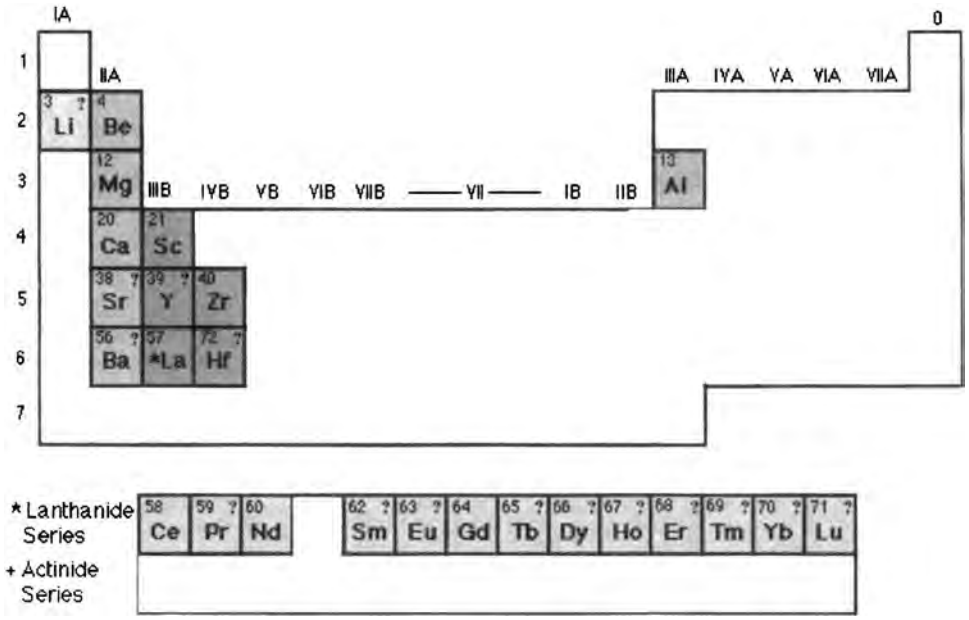


FIG. 120. Elements whose oxides are stable on Si, with respect to the formation of both SiO_2 and MSi_x (silicide), at 1000 K. The question mark indicates lack of thermodynamic data for the silicide of the particular element [adapted from Hubbard *et al.* (Ref. 725)].

A. Si_3N_4

Si_3N_4 has been suggested as an alternative gate dielectric. However, typically its interface properties with Si are poor. Further, it is difficult to fabricate ultrathin films without incorporating some O near the interface,[723] since Si has a greater affinity for O than for N. Indeed, the incorporation of O at the interface may be the reason that high N-containing Si–O–N films have any reasonable electrical properties at all. Some progress has been made in growing electrically acceptable pseudo-Si_3N_4[723] and Si_3N_4[530] films but since the dielectric constant, even for the best case of pure Si_3N_4, is only twice that of SiO_2, it may be preferable to use metal oxides, some of which have much higher dielectric constants. If the interface properties of Si_3N_4 are perfected, it may be useful as an interim gate dielectric solution.

B. Alternate (higher) dielectric constant materials

Table VIII is a list of requirements for alternate gate dielectrics. We will use this table to frame our discussion. A more comprehensive treatment of high-κ gate dielectrics will be found in a companion review article.[724] Alternate gate dielectric materials must meet a variety of chemical, physical, electrical, and manufacturing criteria. The gate dielectric must be thermodynamically stable on Si, with respect to the formation of both SiO_2 and MSi_x. At the appropriate process temperatures to which the wafer will be exposed, Si should not reduce the gate dielectric to form SiO_2 or silicide. If SiO_2 were formed, the capacitance ''budget'' would be consumed by a low dielectric constant material. If the silicide were formed, a conductive path across the channel might be created. Stability criteria for all simple, as well as some multicomponent metal oxides, have been thoroughly explored.[725] The imposition of the thermodynamic stability criteria substantially reduces the field of acceptable alternate gate dielectrics. Figure 120 shows the elements whose oxides are thermodynamically stable on Si, at 1000 K, with respect to both SiO_2 or silicide formation.

Table IX is a partial list of candidate high-κ materials suggested by Fig. 120. No simple oxide seems to have the right combination of dielectric constant, thermodynamic stability on Si, and stability of the amorphous phase at reasonable processing temperatures. Zirconium, and other metals including notably Ti, will readily form silicides if the processing ambient is not controlled properly.[206] Al_2O_3 has a reasonable dielectric constant, and has therefore been the

TABLE IX. Some candidate high-κ simple metal oxides.

	SiO_2	Al_2O_3	ZrO_2	HfO_2	TiO_2	Ta_2O_5
Dielectric constant	3.9	9.5	22	20	80	25
Band gap, eV	9	8.8	4	4.5	3	5
Free energy of reaction: $Si+MO_x \rightarrow M+SiO_2$ at 727 °C, kcal/mole of MO_x		63.4	42.3	47.6	7.5	−52.5
Stability of amorphous phase	high	high	low	low	high	low
Silicide phase formation possible?		no	yes	yes	yes	yes
Oxygen diffusivity at 950 °C, cm^2/s	2×10^{-14}	5×10^{-25}	10^{-12}	?	10^{-13}	?

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

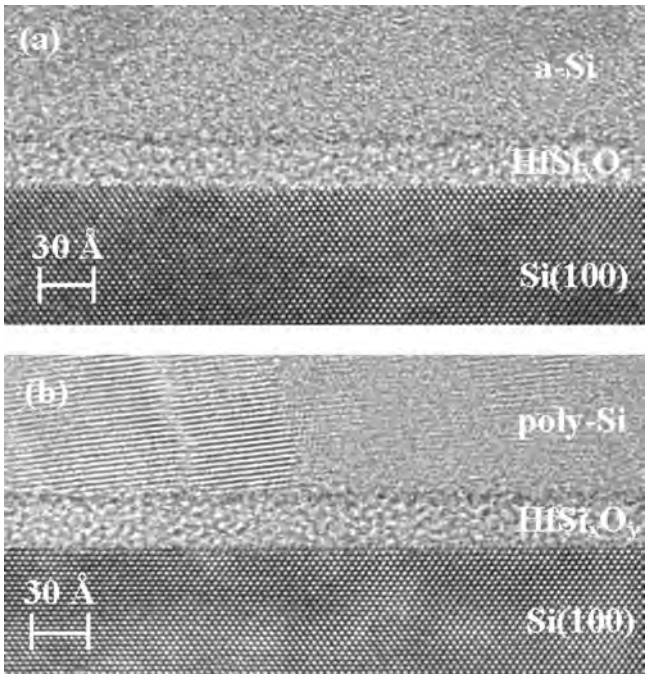


FIG. 121. TEM cross section of a ~30 Å $Hf_7Si_{29}O_{64}$ film with a Si cap (a) as-deposited at 500 °C and (b) after annealing at 1050 °C for 20 sec in N_2. The amorphous Si cap crystallized during the anneal, but the dielectric film remained amorphous and stable, while maintaining atomically sharp interfaces with both the substrate and the cap layer [from Wilk *et al.* (Ref. 730)].

subject of considerable research.[207,726–728] Since SiO_2 and Al_2O_3 have very stable amorphous phases, silicates[729–731] and aluminates[732,733] may be promising candidates. It should be mentioned that some metal oxides, not stable on Si, e.g., Ta_2O_5, may be suitable with the use of a barrier layer, or due to the slow kinetics of the reaction, with the Si substrate. For that reason, Ta_2O_5 is included in Table IX; however, the use of these materials involves compromises that will not lead to the most robust solutions for high-κ gate materials.

Clearly, amorphous gate dielectrics (as is SiO_2), offer many benefits and are the most desirable. However, most metal oxides exhibit a strong tendency to crystallize. It remains to be seen to what extent some degree of crystallinity may degrade the reliability of metal oxides. Figure 121 is an example of amorphous phase stability in a silicate phase.[729] SiO_2 readily forms a stable amorphous phase due to the SiO_4 tetrahedral subunits that comprise it. Methods of stabilizing the amorphous phases, either through the formation of silicates, or other alloying schemes,[733] may have to be found. The microstructure of the dielectric layer plays a significant role in its performance. Polycrystalline dielectrics are not desirable because grain boundaries will facilitate mass and electrical transport, and thereby adversely affect reliability. Crystallization may also give rise to interfacial roughness, which will lower channel mobility. Although epitaxial dielectrics have been demonstrated,[734] and promise very low defect density interfaces, they too present problems. The requirement for an epitaxial match reduces the field of possible candidates yet further. Also, the domain boundaries in the epitaxial dielectric that will result from growth on the stepped Si surface may behave just like grain boundaries. Further, epitaxial dielectrics will have anisotropic properties, not necessarily desirable. Finally, commercial growth techniques for epitaxy of these materials would have to be developed.

From an electrical standpoint, the dielectric constant of the alternate gate dielectric should be ~9–25. If the dielectric constant is too high, the gate dielectric layer will be too thick relative to the channel dimensions, and fringing field effects will affect performance.[735,736] The dielectric should also have a large band gap, so that gate leakage current may be minimized. Few alternate gate dielectric materials have band gaps approaching that of SiO_2, 9.0 eV, but the thicker gate dielectric layer (compared to its SiO_2 equivalent) will also result in lower leakage current. Further, the gate dielectric should form a high quality, low defect density ($<5\times10^{10}\,cm^{-2}\,eV^{-1}$) interface with Si. There are many other considerations that must be taken into account when selecting a high-κ material, including etchability, O diffusivity, and electronic defect structure. These will not be known in detail until the field of candidates has been narrowed down.

Processing requirements for alternate gate dielectrics are also important. Without a manufacturable process, high-κ materials will never be introduced into technology. It is very critical that adventitious SiO_2 not be formed during alternate gate dielectric growth. Although a few monolayers of SiO_2 at the interface might prove beneficial for good interface properties, a thicker layer of this low dielectric constant material would not allow for the growth of an alternate gate dielectric with t_{ox}(eq) of <1.0 nm. Reactive sputtering in particular results in an adventitious SiO_2 layer at least 1.5 nm thick,[726] and is not a suitable deposition technique. Low pressure CVD,[727,737,738] atomic layer deposition (ALD),[739] and molecular beam epitaxy (MBE),[734] all of which have the potential for growth with sufficient interface control, are candidates for deposition of the alternate gate dielectrics. Of these, MBE may be the most problematic in that this technique has not made commercial inroads in Si processing. Further, in the future new gate formation (''replacement gate'') technologies[740,741] might be used to make integrated devices. Conformal film coverage will be of paramount importance for such technologies, since nonplanar topographies will be introduced, and processes such as ALD[206,207,512,739,742] or LPCVD[738] will be required.

ACKNOWLEDGMENTS

The authors gratefully acknowledge helpful discussions and comments from D. A. Buchanan, E. Cartier, T. W. Sorsch, J. H. Stathis, and B. E. Weir.

[1] L. Feldman, E. P. Gusev, and E. Garfunkel, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 1.
[2] E. P. Gusev, H. C. Lu, E. Garfunkel, T. Gustafsson, and M. Green, IBM J. Res. Dev. **43**, 265 (1999).
[3] R. Degraeve, B. Kaczer, and G. Groeseneken, Microelectron. Reliab. **39**, 1445 (1999).
[4] G. Timp, R. E. Howard, and P. M. Mankiewich, in *Nanotechnology*, edited by G. Timp (Springer-Verlag, New York, 1998), p. 7.
[5] G. E. Moore, Electron. Mag. **38**, 114 (1965).
[6] R. R. Schaller, IEEE Spectrum **34**, 52 (1997).
[7] P. Peercy, Nature (London) **406**, 1042 (2000).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[8] R. D. Isaac, IBM J. Res. Dev. **44**, 369 (2000).
[9] R. Chau, J. Kavaleiros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murthy, and G. Dewey, Tech. Dig. Int. Electron Devices Meet. **2000**, 45.
[10] G. Timp, A. Agarwal, F. H. Baumann, T. Boone, M. Buonanno, R. Cirelli, V. Donelly, M. Foad, D. Grant, M. L. Green, H. Gossmann, S. Hillenius, J. Jackson, D. Jacobson, R. Kleiman, A. Kornblit, F. Klemens, J. T.-C. Lee, W. Mansfield, S. Moccio, A. Murrell, M. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W. W. Tai, D. Tennant, H. Vuong, and B. Weir, Tech. Dig. Int. Electron Devices Meet. **1997**, 930.
[11] Y. Taur, D. Buchanan, W. Chen, D. J. Frank, K. I. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H.-J. C. Wann, S. J. Wind, and H.-S. Wong, Proc. IEEE **85**, 486 (1997).
[12] A. Chaterjee, R. A. Chapman, G. Dixit, J. Kuehne, S. Hattangady, H. Yang, G. A. Brown, R. Aggarwal, U. Erdogan, Q. He, M. Hanratty, D. Rogers, S. Murtaza, S. J. Fang, R. Kraft, A. L. P. Rotondaro, J. C. Hu, M. Terry, W. Lee, C. Fernando, A. Konecni, G. Wells, D. Frystak, C. Bowen, M. Rodder, and I.-C. Chen, Tech. Dig. Int. Electron Devices Meet. **1997**, 821.
[13] G. Timp, K. K. Bourdelle, J. E. Bower, F. H. Baumann, T. Boone, R. Cirelli, K. Evans-Lutterodt, J. Garno, A. Ghetti, H. Gossmann, M. L. Green, D. Jacobson, Y. Kim, R. Kleiman, F. Klemens, A. Kornblit, C. Lochstampfor, W. Mansfield, S. Moccio, D. A. Muller, L. E. Ocola, M. L. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, D. M. Tennant, W. Timp, and B. E. Weir, Tech. Dig. Int. Electron Devices Meet. **1998**, 615.
[14] G. Timp, A. Agarwal, K. K. Bourdelle, J. E. Bower, T. Boone, A. Ghetti, M. L. Green, J. Garno, H. Gossmann, D. Jacobson, R. Kleiman, A. Kornblit, F. Klemens, S. Moccio, M. L. O'Malley, L. Ocola, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W. Timp, and D. Tennant, Tech. Dig. Int. Electron Devices Meet. **1998**, 1041.
[15] G. Timp, J. Bude, K. K. Bourdelle, J. Garno, A. Ghetti, H. Gossmann, M. L. Green, G. Forsyth, Y. Kim, R. Kleiman, F. Klemens, A. Kornblit, C. Lochstampfor, W. Mansfield, S. Moccio, T. Sorsch, D. M. Tennant, W. Timp, and R. Tung, Tech. Dig. Int. Electron Devices Meet. **1999**, 55.
[16] *International Technology Roadmap for Semiconductors* (Semiconductor Industry Association, San Jose, CA, 1999).
[17] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, Nature (London) **399**, 758 (1999).
[18] *The Physics and Chemistry of Si and the Si/SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1988), Vol. I.
[19] *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1993), Vol. II.
[20] *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface*, edited by H. Z. Massoud, E. H. Poindexter, and C. R. Helms (Electrochemical Society, Pennington, NJ, 1996), Vol. III.
[21] P. Balk, *The Si-SiO_2 System* (Elsevier, Amsterdam, 1988).
[22] T. Hori, *Gate Dielectrics and MOS ULSI* (Springer, Berlin, 1997).
[23] E. Y. J. Chabal, *Fundamental Aspects of Silicon Oxidation* (Springer-Verlag, Berlin, 2001), Vol. 46.
[24] P. Balk, Adv. Mater. **7**, 703 (1995).
[25] I. J. R. Baumvol, Surf. Sci. Rep. **36**, 1 (1999).
[26] T. Engel, Surf. Sci. Rep. **18**, 91 (1993).
[27] M. P. D'Evelyn, M. M. Nelson, and T. Engel, Surf. Sci. **186**, 75 (1987).
[28] C. J. Sofield and A. M. Stoneham, Semicond. Sci. Technol. **10**, 215 (1995).
[29] E. Irene, Crit. Rev. Solid State Mater. Sci. **14**, 175 (1988).
[30] R. B. Fair, J. Electrochem. Soc. **128**, 1360 (1981).
[31] C. R. Helms and E. H. Poindexter, Rep. Prog. Phys. **57**, 791 (1994).
[32] W. B. Fowler, Rev. Solid State Sci. **5**, 435 (1991).
[33] E. H. Poindexter, Semicond. Sci. Technol. **4**, 961 (1989).
[34] W. Weber and M. Brox, MRS Bull. **12**, 36 (1993).
[35] C. Hu, Proc. IEEE **81**, 682 (1993).
[36] A. C. Diebold, D. Venables, Y. Chabal, D. Muller, M. Weldon, and E. Garfunkel, Mater. Sci. Semicond. Process. **2**, 103 (1999).
[37] F. H. P. M. Habraken and A. E. T. Kuiper, Mater. Sci. Eng., R. **R12**, 123 (1994).
[38] M. M. Moslehi and K. C. Saraswat, IEEE Trans. Electron Devices **ED-32**, 106 (1985).
[39] E. P. Gusev, in *Defects in SiO_2 and Related Dielectrics: Science and Technology*, edited by G. Pacchioni (Kluwer, Dordrecht, 2000), pp. 557–579.
[40] D. Buchanan, IBM J. Res. Dev. **43**, 245 (1999).
[41] *Silicon and Siliceous Structures in Biological Systems* (Springer-Verlag, Berlin, 1981).
[42] H. A. Lowenstam and S. Weiner, *On Biomineralization* (Oxford University, New York, 1989).
[43] G. A. Ozin, Acc. Chem. Res. **30**, 17 (1997).
[44] H. Yang, N. Coombs, I. Sokolov, and G. A. Ozin, Nature (London) **381**, 589 (1996).
[45] M. L. Green, T. W. Sorsch, G. L. Timp, D. A. Muller, B. E. Weir, P. J. Silverman, S. V. Moccio, and Y. O. Kim, Microelectron. Eng. **48**, 25 (1999).
[46] S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, IEEE Electron Device Lett. **ED-18**, 209 (1997).
[47] T. Yoshida, D. Imafuku, J. L. Alay, S. Miyazaki, and M. Hirose, Jpn. J. Appl. Phys., Part 2 **34**, L903 (1995).
[48] A. Schenk and G. Heiser, J. Appl. Phys. **81**, 7900 (1997).
[49] M. S. Krishnan, L. Chang, T.-J. King, J. Bokor, and C. Hu, Tech. Dig. Int. Electron Devices Meet. **1999**, 241.
[50] M. V. Fischetti and S. E. Laux, Appl. Phys. Lett. **76**, 2277 (2000).
[51] T. Matsuoka, S. Taguchi, K. Taniguchi, C. Hamaguchi, S. Kakimoto, and J. Takagi, IEICE Trans. Electron. **E78-C**, 248 (1995).
[52] T. P. Ma, Nucl. Instrum. Methods Phys. Res. B **74**, 295 (1993).
[53] R. Degraeve, P. Roussel, G. Groeseneken, and H. E. Maes, Microelectron. Reliab. **36**, 1639 (1996).
[54] J. H. Stathis and D. J. DiMaria, Tech. Dig. Int. Electron Devices Meet. **1998**, 167.
[55] J. H. Stathis, Microelectron. Eng. **36**, 325 (1997).
[56] D. J. DiMaria, Microelectron. Eng. **36**, 317 (1997).
[57] M. Depas and M. M. Heyns, Microelectron. Eng. **36**, 21 (1997).
[58] A. Toriumi, H. Satake, N. Yasuda, and T. Tanamoto, Appl. Surf. Sci. **117-118**, 230 (1997).
[59] R. Degraeve, J. L. Ogier, R. Bellens, P. Rousel, G. Groeseneken, and H. E. Maes, Proc. IEEE Int. Reliability Phys. Symp. 1996, p. 44.
[60] D. A. Buchanan and S. H. Lo, Microelectron. Eng. **36**, 13 (1997).
[61] B. E. Weir, P. J. Silverman, D. Monroe, K. S. Krisch, M. A. Alam, G. B. Alers, T. W. Sorsch, G. L. Timp, F. Baumann, C. T. Liu, Y. Ma, and D. Hwang, Tech. Dig. Int. Electron Devices Meet. **1997**, 73.
[62] B. E. Weir, M. A. Alam, J. D. Bude, P. J. Silverman, A. Ghetti, F. Baumann, P. Diodato, D. Monroe, T. Sorsch, G. L. Timp, Y. Ma, M. M. Brown, A. Hamad, D. Hwang, and P. Mason, Semicond. Sci. Technol. **15**, 455 (2000).
[63] D. A. Buchanan and D. J. DiMaria, J. Appl. Phys. **67**, 7439 (1990).
[64] E. Cartier, D. J. DiMaria, D. A. Buchanan, J. H. Stathis, W. W. Abadeer, and R. R. Vollersten, IEEE Trans. Electron Devices **ED-99**, 1234 (1994).
[65] D. A. Buchanan, A. D. Marwick, D. J. DiMaria, and L. Dori, J. Appl. Phys. **76**, 3595 (1994).
[66] M. Alam, J. Bude, B. Weir, P. Silverman, A. Ghetti, D. Monroe, K. P. Cheung, and S. Moccio, Tech. Dig. Int. Electron Devices Meet. **1999**, 715.
[67] C. T. Liu, Y. Ma, M. Oh, P. W. Diodato, K. R. Stiles, J. R. McMacken, F. Li, C. P. Chang, K. P. Cheung, J. I. Colonell, W. Y. C. Lai, R. Liu, E. J. Lloyd, J. F. Miner, C. S. Pai, H. Vaidya, J. Fracoviak, A. Timko, F. Klemens, H. Maynard, and J. T. Clemens, Tech. Dig. Int. Electron Devices Meet. **1998**, 589.
[68] Y.-C. King, C. Kuo, T.-J. King, and C. Hu, Tech. Dig. Int. Electron Devices Meet. **1998**, 585.
[69] J. M. Hergenrother, D. Monroe, F. P. Klemens, A. Kornblit, G. R. Weber, W. M. Mansfield, M. R. Baker, F. H. Baumann, K. J. Bolan, J. E. Bower, N. A. Ciampa, R. A. Cirelli, J. I. Colonell, D. J. Eaglesham, J. Fracoviak, H. J. Gossmann, M. L. Green, S. J. Hillenius, C. A. King, R. N. Kleiman, W. Y.-C. Lai, J. T.-C. Lee, R. C. Liu, H. L. Maynard, M. D. Morris, S.-H. Oh, C.-S. Pai, C. S. Rafferty, J. M. Rosamilia, T. W. Sorsch, and H.-H. Vuong, Tech. Dig. Int. Electron Devices Meet. **1999**, 75.
[70] D. E. Aspnes and J. B. Theeten, Phys. Rev. Lett. **43**, 1046 (1979).
[71] J. B. Theeten, D. E. Aspnes, F. Simondet, M. Erman, and P. C. Mürau, J. Appl. Phys. **52**, 6788 (1981).
[72] E. Irene, Thin Solid Films **233**, 96 (1993).
[73] H. Z. Massoud, J. D. Plummer, and E. A. Irene, J. Electrochem. Soc. **132**, 1745 (1985).
[74] Q. Liu, J. F. Wall, and E. A. Irene, J. Vac. Sci. Technol. A **12**, 2625 (1994).
[75] V. A. Yakovlev, Q. Liu, and E. Irene, J. Vac. Sci. Technol. A **10**, 427 (1992).
[76] G. E. Jellison, J. Appl. Phys. **69**, 7627 (1991).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[77] E. A. Irene and Y. J. van der Meulen, J. Electrochem. Soc. **123**, 1380 (1976).
[78] S. Y. Kim and E. A. Irene, Rev. Sci. Instrum. **66**, 5277 (1995).
[79] N. M. Ravindra, J. Narayan, D. Fathy, J. K. Stivastava, and E. A. Irene, J. Mater. Res. **2**, 216 (1987).
[80] C. H. An and K. Sugimoto, J. Electrochem. Soc. **141**, 853 (1994).
[81] R. H. Doremus and S. C. Kao, in *Interface Control of Electrical, Chemical, and Mechanical Properties; Vol. 318*, edited by S. P. Murarka, K. Rose, T. Ohmi, and T. Seidel (Materials Research Society, Pittsburgh, 1994), p. 53.
[82] T. S. Chao, Jpn. J. Appl. Phys., Part 1 **34**, 2370 (1995).
[83] N. Gonon, A. Gagnaire, D. Barbier, and A. Glachant, J. Appl. Phys. **76**, 5242 (1994).
[84] K. Utani and S. Adachi, Jpn. J. Appl. Phys., Part 1 **32**, 3572 (1993).
[85] N. V. Nguyen, D. Chandler-Horowitz, P. M. Amirtharaj, and J. G. Pellegrino, Appl. Phys. Lett. **64**, 2688 (1994).
[86] G. P. M. Poppe, H. Wormeester, A. Molenbroek, C. M. J. Wijers, and A. VanSilfhout, Phys. Rev. B **43**, 12122 (1991).
[87] T. Yasuda, L. Mantese, U. Rossow, and D. E. Aspnes, Phys. Rev. Lett. **74**, 3431 (1995).
[88] B. Drevillon and V. Yakovlev, in *Physics of Thin Films: Optical Characterization of Real Surfaces and Films*, edited by K. Vedam (Academic New York, 1994), p. 1.
[89] C. H. Bjorkman, C. E. Shearon, Jr., Y. Ma, T. Yasuda, G. Lucovsky, U. Emmerichs, C. Meyer, K. Leo, and H. Kurz, J. Vac. Sci. Technol. A **11**, 964 (1993).
[90] J. I. Dadap, B. Doris, Q. Deng, M. C. Downer, J. K. Lowell, and A. C. Diebold, Appl. Phys. Lett. **64**, 2139 (1994).
[91] J. I. Dadap, X. F. Hu, M. H. Anderson, M. C. Downer, J. K. Lowell, and O. A. Aktsipetrov, Phys. Rev. B **53**, R7607 (1996).
[92] G. Lucovsky, Phys. Rev. B **49**, 14003 (1994).
[93] J. F. McGlip, J. Phys. D **29**, 1812 (1996).
[94] C. Meyer, G. Lupke, U. Emmerichs, F. Wolter, H. Kurz, C. H. Bjorkman, and G. Lucovsky, Phys. Rev. Lett. **74**, 3001 (1995).
[95] K. Nakamura, A. Kurokawa, and S. Ichimura, J. Vac. Sci. Technol. A **15**, 2441 (1997).
[96] G. Lupke, D. J. Bottomley, and H. M. v. Driel, Phys. Rev. B **47**, 10389 (1993).
[97] J. Fang and G. P. Li, Appl. Phys. Lett. **75**, 3506 (1999).
[98] Y. J. Chabal, Phys. Rev. Lett. **53**, 282 (1984).
[99] Y. J. Chabal, Prog. Surf. Sci. **48**, 313 (1995).
[100] Y. J. Chabal, Surf. Sci. **380**, 444 (1997).
[101] T. S. Chao, W. H. Chen, and T. F. Lei, Jpn. J. Appl. Phys., Part 1 **34**, 2370 (1995).
[102] A. C. Dillon, S. M. George, and P. Gupta, J. Electron Spectrosc. Relat. Phenom. **54/54**, 1085 (1990).
[103] G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson, and R. S. Urdahl, Appl. Phys. Lett. **73**, 1517 (1998).
[104] M. K. Weldon, K. T. Queeney, Y. J. Chabal, B. B. Stefanov, and K. Raghavachari, J. Vac. Sci. Technol. B **17**, 1795 (1999).
[105] T. Yamazaki, S. Miyazaki, C. H. Bjorkman, M. Fukuda, and M. Hirose, in *Interface Control of Electrical, Chemical, and Mechanical Properties*, edited by S. P. Murarka, K. Rose, T. Ohmi, and T. Seidel (Materials Research Society, Pittsburgh, 1994), Vol. 318, p. 419.
[106] C. H. Bjorkman, T. Yamazaki, S. Miyazaki, and M. Hirose, J. Appl. Phys. **77**, 313 (1995).
[107] H. Ono and K. Koyanagi, Appl. Phys. Lett. **75**, 3521 (1999).
[108] Z. H. Lu, J. P. McCaffrey, B. Brar, G. D. Wilk, R. M. Wallace, L. C. Feldman, and S. P. Tay, Appl. Phys. Lett. **71**, 2764 (1997).
[109] K. J. Hebert, S. Zafar, E. A. Irene, R. Kuehn, J. E. McCarthy, and E. K. Demirlioglu, Appl. Phys. Lett. **68**, 266 (1996).
[110] K. J. Hebert, T. Labayen, and E. A. Irene, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface-3*, edited by H. Z. Massoud, E. H. Poindexter, and C. R. Helms (Electrochemical Society, Pennington, NJ, 1996), p. 81.
[111] D. M. Brown, P. V. Gray, F. K. Heumann, H. R. Philipp, and E. A. Taft, J. Electrochem. Soc. **115**, 311 (1968).
[112] V. A. Gritsenko, *Structure and Electronic Properties of Amorphous Insulators in Silicon MIS Structures* (Science, Novosibirsk, Russia, 1993).
[113] E. A. Irene, Q. Liu, W. M. Paulson, P. J. Tobin, and R. I. Hedge, J. Vac. Sci. Technol. B **14**, 1697 (1996).
[114] R. A. B. Devine, J. Vac. Sci. Technol. A **6**, 3154 (1988).
[115] R. A. B. Devine, Appl. Phys. Lett. **68**, 3108 (1996).
[116] Y. J. Chabal, J. Vac. Sci. Technol. A **3**, 1448 (1985).
[117] Y. J. Chabal, Physica B **170**, 447 (1991).
[118] Y. J. Chabal, Surf. Sci. **168**, 594 (1986).
[119] K. T. Queeney, M. K. Weldon, J. P. Chang, Y. J. Chabal, A. B. Gurevich, J. Sapjeta, and R. L. Opila, J. Appl. Phys. **87**, 1322 (2000).
[120] H. Ono, T. Ikarashi, Y. Miura, E. Hasegawa, K. Ando, and T. Kitano, Appl. Phys. Lett. **74**, 203 (1999).
[121] S. I. Raider and R. Flitsch, IBM J. Res. Dev. **22**, 294 (1978).
[122] F. J. Grunthaner and P. J. Grunthaner, Mater. Sci. Rep. **1**, 65 (1986).
[123] F. G. Himpsel, Surf. Sci. **299/300**, 525 (1994).
[124] T. Hattori, CRC Crit. Rev. Solid State Mater. Sci. **20**, 339 (1995).
[125] S. Iwata and A. Ishizaka, J. Appl. Phys. **79**, 6653 (1996).
[126] Z. H. Lu, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 49.
[127] F. J. Grunthaner, P. J. Grunthaner, R. P. Vasquez, B. F. Lewis, J. Maserjian, and A. Madhukar, Phys. Rev. Lett. **43**, 1683 (1979).
[128] C. Maillot, H. Roulet, and G. Dufour, J. Vac. Sci. Technol. B **2**, 316 (1984).
[129] P. J. Grunthaner, M. H. Hecht, F. J. Grunthaner, and N. M. Johnson, J. Appl. Phys. **61**, 629 (1987).
[130] F. J. Himpsel, F. R. McFeely, A. Taleb-Ibrahimi, J. A. Yarmoff, and G. Hollinger, Phys. Rev. B **38**, 6084 (1988).
[131] J. L. Bischoff, Surf. Sci. **209**, 115 (1989).
[132] M. Niwano, H. Katakura, Y. Takeda, Y. Takakuwa, N. Miyamoto, A. Hiraiwa, and K. Yagi, J. Vac. Sci. Technol. A **9**, 195 (1991).
[133] M. M. Banaszak-Holl and F. R. McFeely, Phys. Rev. Lett. **71**, 2441 (1993).
[134] Z. H. Lu, M. J. Graham, D. T. Jiang, and K. H. Tan, Appl. Phys. Lett. **63**, 2941 (1993).
[135] E. C. Carr and R. A. Buhrman, Appl. Phys. Lett. **63**, 54 (1993).
[136] M. M. Banaszak-Holl, S. Lee, and F. R. McFeely, Appl. Phys. Lett. **65**, 1097 (1994).
[137] Z. H. Lu, S. P. Tay, R. Cao, and P. Pianetta, Appl. Phys. Lett. **67**, 2836 (1995).
[138] M. T. Seiger, D. A. Luh, T. Miller, and T. C. Chiang, Phys. Rev. Lett. **77**, 2758 (1996).
[139] K. Z. Zhang, M. M. Banaszak-Holl, J. E. Bender, S. Lee, and F. R. McFeely, Phys. Rev. B **54**, 7686 (1996).
[140] J. W. Keister, J. E. Rowe, J. J. Kolodziej, H. Niimi, H.-S. Tao, T. E. Madey, and G. Lucovsky, J. Vac. Sci. Technol. A **17**, 1250 (1999).
[141] E. Cartier and F. R. McFeely, Phys. Rev. B **44**, 10689 (1991).
[142] W. M. Lau and X.-W. Wu, Surf. Sci. **245**, 345 (1991).
[143] J. L. Alay and M. Hirose, J. Appl. Phys. **81**, 1606 (1997).
[144] T. Hattori, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), pp. 241–256.
[145] J. W. Keister, J. E. Rowe, J. J. Kolodziej, H. Niimi, T. E. Madey, and G. Lucovsky, J. Vac. Sci. Technol. B **17**, 1831 (1999).
[146] V. D. Borman, E. P. Gusev, Y. Y. Lebedinski, and V. I. Troyan, Phys. Rev. Lett. **67**, 2387 (1991).
[147] V. D. Borman, E. P. Gusev, Y. Y. Lebedinski, and V. I. Troyan, Phys. Rev. B **49**, 5415 (1994).
[148] A. Namiki and K. Tanimoto, Surf. Sci. **222**, 530 (1989).
[149] F. Lutz, L. Kubler, J. L. Bischoff, and D. Bolmont, Phys. Rev. B **40**, 11747 (1989).
[150] P. Morgen, U. Hoffer, W. Wurth, and E. Umbach, Phys. Rev. B **39**, 3720 (1989).
[151] Z. Nakazawa and H. Sekiyama, Appl. Phys. Lett. **56**, 2108 (1990).
[152] L. J. Terminello, J. A. Yarmoff, F. M. d'Heurle, and F. R. McFeely, Surf. Sci. **243**, 127 (1991).
[153] H. Yagachi, K. Fujita, S. Fukatsu, Y. Shiraki, R. Ito, T. Igarashi, and T. Hattori, Surf. Sci. **275**, 395 (1992).
[154] F. Lutz, Appl. Surf. Sci. **72**, 427 (1993).
[155] T. Hattori and K. Ohishi, Mat. Res. Soc. Symp. Proc. **318**, 61 (1994).
[156] K. Ohishi and T. Hattori, Jpn. J. Appl. Phys., Part 2 **33**, L675 (1994).
[157] Z. Q. Yao, H. B. Harrison, S. Dimitrijev, Y. T. Yeow, and D. Sweatman, Appl. Phys. Lett. **64**, 3584 (1994).
[158] Z. Q. Yao, J. Appl. Phys. **78**, 2906 (1995).
[159] M. Tabe, T. T. Chiang, I. Lindau, and W. E. Spicer, Phys. Rev. B **34**, 2706 (1986).
[160] M. Tabe and T. Yamamoto, Surf. Sci. **376**, 99 (1997).
[161] G. Hollinger and F. J. Himpsel, Phys. Rev. B **28**, 3651 (1983).
[162] H. Kobayashi, T. Mizokuro, Y. Nakato, K. Yoneda, and Y. Todokoro, Appl. Phys. Lett. **71**, 1978 (1997).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[163] K. Raghavachari and J. Eng, Phys. Rev. Lett. **84**, 935 (2000).
[164] K. S. Schneider, K. Z. Zhang, M. Banasek-Holl, B. G. Orr, and U. C. Pernisz, Phys. Rev. Lett. **85**, 602 (2000).
[165] A. Pasquarello, M. S. Hybertsen, and R. Car, Phys. Rev. Lett. **74**, 1024 (1995).
[166] F. R. McFeely, K. Z. Zhang, M. M. Banaszak-Hall, S. Lee, and J. E. Bender, J. Vac. Sci. Technol. B **14**, 2824 (1996).
[167] K. Z. Zhang, K. E. Litz, M. M. B. Holl, and F. R. McFeely, Appl. Phys. Lett. **72**, 46 (1998).
[168] S. I. Raider, R. A. Gdula, and J. R. Petrak, Appl. Phys. Lett. **27**, 150 (1975).
[169] R. I. Hegde, P. J. Tobin, K. G. Reid, B. Maiti, and S. A. Ajuria, Appl. Phys. Lett. **66**, 2882 (1995).
[170] M. Bhat, L. K. Han, D. Wristers, J. Yan, D. L. Kwong, and J. Fulford, Appl. Phys. Lett. **66**, 1225 (1995).
[171] A. P. Caricato, F. Cazzaniga, G. F. Cerofolini, B. Crivelli, M. L. Polignano, G. Tallarida, S. Valeri, and R. Zonca, in *Ultrathin SiO_2 and High-K Materials for ULSI Gate Dielectrics*, edited by H. R. Huff, C. A. Richter, M. L. Green, G. Lucovsky, and T. Hattori (Materials Research Society, Warrendale, 1999), Vol. 567, p. 135.
[172] J. P. Chang, M. L. Green, V. M. Donnelly, R. L. Opila, J. Eng, J. Sapjeta, P. J. Silverman, B. Weir, H. C. Lu, T. Gustafsson, and E. Garfunkel, J. Appl. Phys. **87**, 4449 (2000).
[173] M. L. Green, D. Brasen, K. W. Evans-Lutterodt, L. C. Feldman, K. Krisch, W. Lennard, H. T. Tang, L. Manchanda, and M. T. Tang, Appl. Phys. Lett. **65**, 848 (1994).
[174] M. T. Tang, K. W. Evans-Lutterodt, G. S. Higashi, and T. Boone, Appl. Phys. Lett. **62**, 3144 (1993).
[175] M. T. Tang, K. W. Evans-Lutterodt, M. L. Green, D. Brasen, K. Krisch, L. Manchanda, G. S. Higashi, and T. Boone, Appl. Phys. Lett. **64**, 748 (1994).
[176] J. A. Dura, C. A. Richter, C. F. Majkrzak, and N. V. Nguyen, Appl. Phys. Lett. **73**, 2131 (1998).
[177] S. D. Kosowsky, C. H. Hsu, P. S. Pershan, J. Bevk, and B. S. Freer, Appl. Surf. Sci. **84**, 179 (1995).
[178] T. A. Rabedeau, I. M. Tidswell, P. S. Pershan, J. Bevk, and B. S. Freer, Appl. Phys. Lett. **59**, 3422 (1991).
[179] E. Hasegawa, A. Ishitani, K. Akimoto, M. Tsukiji, and N. Ohta, J. Electrochem. Soc. **142**, 273 (1995).
[180] N. Awaji, Y. Sugita, T. Nakanishi, S. Ohkubo, K. Takasaki, and S. Komiya, J. Vac. Sci. Technol. A **14**, 971 (1996).
[181] S. Banerjee, Y. J. Park, D. R. Lee, Y. H. Jeong, K.-B. Lee, S. B. Yoon, B. H. Jo, H. M. Choi, and W.-J. Cho, Appl. Phys. Lett. **72**, 433 (1998).
[182] L. Brugemann, R. Bloch, W. Press, and P. Gerlach, J. Phys.: Condens. Matter **2**, 8869 (1990).
[183] I. Hirosawa, K. Akimoto, T. Tatsumi, J. Mizuki, and J. Matsui, J. Cryst. Growth **103**, 150 (1990).
[184] S. D. Kosowsky, P. S. Pershan, K. S. Krisch, J. Bevk, M. L. Green, D. Brasen, L. C. Feldman, and P. K. Roy, Appl. Phys. Lett. **70**, 3119 (1997).
[185] P. H. Fouss, H. J. Norton, S. Brennan, and A. Fisher-Colbrie, Phys. Rev. Lett. **60**, 600 (1988).
[186] G. Renaud, P. H. Fouss, A. Ourmazd, J. Bevk, B. S. Freer, and P. O. Hahn, Appl. Phys. Lett. **58**, 1044 (1991).
[187] G. R. Harp, D. K. Saldin, and B. P. Tonner, J. Phys.: Condens. Matter **5**, 5377 (1993).
[188] A. Munkholm, S. Brennan, F. Comin, and L. Ortega, Phys. Rev. Lett. **75**, 4254 (1995).
[189] I. Takahashi, T. Shimura, and J. Harada, J. Phys.: Condens. Matter **5**, 6525 (1993).
[190] J. L. Jordan-Sweet, R. Ludeke, T. B. Hook, and K. W. Evans-Lutterodt, Adv. X-Ray Anal. **41**, 1999 (International Center for Diffraction Data, CD-ROM).
[191] S. T. Cundiff, W. H. Knox, F. H. Baumann, K. W. Evans-Lutterodt, M.-T. Tang, and M. L. Green, Appl. Phys. Lett. **70**, 1414 (1997).
[192] L. C. Feldman, J. W. Mayer, and S. T. Picraux, *Materials Analysis by Ion Channeling* (Academic, New York, 1982).
[193] L. C. Feldman, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1988), p. 199.
[194] R. Haight and L. C. Feldman, J. Appl. Phys. **53**, 4884 (1982).
[195] T. E. Jackman, J. R. MacDonald, L. C. Feldman, P. J. Silverman, and I. Stensgaard, Surf. Sci. **100**, 35 (1980).
[196] R. M. Tromp and E. J. van Loenen, Surf. Sci. **155**, 441 (1985).
[197] R. Tromp, G. W. Rubloff, P. Balk, F. K. DeGoues, and E. J. van Loenen, Phys. Rev. Lett. **55**, 2332 (1985).
[198] M. Copel and R. M. Tromp, Rev. Sci. Instrum. **64**, 3147 (1993).
[199] E. P. Gusev, H. C. Lu, T. Gustafsson, and E. Garfunkel, Phys. Rev. B **52**, 1759 (1995).
[200] H. C. Lu, T. Gustafsson, E. P. Gusev, and E. Garfunkel, Appl. Phys. Lett. **67**, 1742 (1995).
[201] H. C. Lu, E. P. Gusev, T. Gustafsson, E. Garfunkel, M. L. Green, D. Brasen, and L. C. Feldman, Appl. Phys. Lett. **69**, 2713 (1996).
[202] E. P. Gusev, H. C. Lu, T. Gustafsson, and E. Garfunkel, in *New Features of Silicon Oxidation in the Ultrathin Regime: An Ion Scattering Study* (Electrochemical Society, Pennington, NJ, 1996), pp. 49–58.
[203] E. P. Gusev, H. C. Lu, T. Gustafsson, E. Garfunkel, M. L. Green, and D. Brasen, J. Appl. Phys. **82**, 896 (1997).
[204] E. Garfunkel, E. P. Gusev, H. C. Lu, T. Gustafsson, and M. L. Green, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 39.
[205] M. Copel, P. R. Varekamp, D. W. Kisker, F. R. McFeely, K. E. Litz, and M. M. Banaszak-Holl, Appl. Phys. Lett. **74**, 1830 (1999).
[206] M. Copel, M. Gribelyuk, and E. P. Gusev, Appl. Phys. Lett. **76**, 436 (2000).
[207] E. P. Gusev, M. Copel, E. Cartier, I. J. R. Baumvol, C. Krug, and M. Gribelyuk, Appl. Phys. Lett. **76**, 176 (2000).
[208] H. C. Lu, N. Yasuda, E. Garfunkel, T. Gustafsson, J. P. Chang, R. L. Opila, and G. B. Alers, Microelectron. Eng. **48**, 287 (1999).
[209] H. Hibino, K. Sumitomo, T. Fukuda, Y. Homma, and T. Ogino, Phys. Rev. B **58**, 12587 (1998).
[210] E. Rosencher, A. Straboni, S. Rigo, and G. Amsel, Appl. Phys. Lett. **34**, 254 (1979).
[211] F. Rochet, B. Agius, and S. Rigo, J. Electrochem. Soc. **131**, 914 (1984).
[212] F. Rochet, S. Rigo, M. Froment, C. d'Anterroches, C. Maillot, H. Roulet, and G. Dufour, Adv. Phys. **35**, 339 (1986).
[213] I. Trimaille and S. Rigo, Appl. Surf. Sci. **39**, 65 (1989).
[214] J. J. Ganem, G. Battistig, S. Rigo, and I. Trimaille, Appl. Surf. Sci. **65/66**, 647 (1993).
[215] I. J. R. Baumvol, J. Electrochem. Soc. **142**, 1205 (1995).
[216] I. J. R. Baumvol and C. Rolfs, Nucl. Instrum. Methods Phys. Res. B **99**, 431 (1995).
[217] J. J. Ganem, S. Rigo, I. Trimaille, I. J. R. Baumvol, and F. C. Stedile, Appl. Phys. Lett. **68**, 2366 (1996).
[218] I. J. R. Baumvol, F. C. Stedile, J. J. Ganem, I. Trimaille, and S. Rigo, J. Electrochem. Soc. **143**, 1426 (1996).
[219] I. J. R. Baumvol, F. C. Stedile, J. J. Ganem, I. Trimaille, and S. Rigo, Appl. Phys. Lett. **70**, 2007 (1997).
[220] I. J. R. Baumvol, F. C. Stedile, C. Radtke, F. L. Freire, E. P. Gusev, M. L. Green, and D. Brasen, Nucl. Instrum. Methods **136-138**, 204 (1998).
[221] I. J. R. Baumvol, E. P. Gusev, F. C. Stedile, F. L. Freire, M. L. Green, and D. Brasen, Appl. Phys. Lett. **72**, 450 (1998).
[222] E. P. Gusev, D. A. Buchanan, P. Jamison, T. H. Zabel, and M. Copel, Microelectron. Eng. **48**, 67 (1999).
[223] I. J. R. Baumvol, C. Krug, F. C. Stedile, F. Gorris, and W. H. Schulte, Phys. Rev. B **60**, 1492 (1999).
[224] T. Åkermark, L. G. Gosset, J.-J. Ganem, I. Trimaille, I. Vickridge, and S. Rigo, J. Appl. Phys. **86**, 1153 (1999).
[225] F. H. P. M. Habraken, E. H. C. Ullersma, W. H. Arnoldbik, and A. E. T. Kuiper, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. P. G. E. Garfunkel and A. Ya. Vul' (Kluwer, Dordrecht, 1998), p. 411.
[226] A. E. T. Kuiper, H. G. Pomp, P. M. Asveld, W. A. Bik, and F. H. P. M. Habraken, Appl. Phys. Lett. **61**, 1031 (1992).
[227] M. R. Frost and C. W. Magee, Appl. Surf. Sci. **104/105**, 379 (1996).
[228] C. J. Han and C. R. Helms, J. Electrochem. Soc. **135**, 1824 (1988).
[229] N. M. Johnson, D. K. Biegelsen, M. D. Moyer, V. R. Deline, and J. C. A. Evans, Appl. Phys. Lett. **38**, 995 (1981).
[230] S. D. Littlewood and J. A. Kilner, J. Appl. Phys. **63**, 2173 (1988).
[231] K. Muraoka, S. Takagi, and A. Toriumi, Extended Abstracts of the 14th International Conference on Solid State Devices and Materials (Business Center for Academic Studies, 1996), p. 500.
[232] J. A. Costello and R. E. Tressler, J. Electrochem. Soc. **131**, 1944 (1984).
[233] N. S. Saks, D. I. Ma, and W. B. Fowler, Appl. Phys. Lett. **67**, 374 (1995).
[234] D. G. J. Sutherland, H. Akatsu, M. Copel, F. J. Himpsel, T. Callcott, J. A. Carlisle, D. Ederer, J. J. Jia, I. Jimenez, R. Perera, D. K. Shuh, L. J. Terminello, and W. M. Tong, J. Appl. Phys. **78**, 6761 (1995).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[235] M. Copel, R. M. Tromp, H. J. Timme, K. Penner, and T. Nakao, J. Vac. Sci. Technol. A **14**, 462 (1996).
[236] M. L. Green, D. Brasen, L. Feldman, E. Garfunkel, E. P. Gusev, T. Gustafsson, W. N. Lennard, H. C. Lu, and T. Sorsch, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 181.
[237] H. C. Lu, E. P. Gusev, T. Gustafsson, M. L. Green, D. Brasen, and E. Garfunkel, Microelectron. Eng. **36**, 29 (1997).
[238] H. C. Lu, E. P. Gusev, T. Gustafsson, and E. Garfunkel, J. Appl. Phys. **81**, 6992 (1997).
[239] M. Copel and R. M. Tromp, Phys. Rev. Lett. **72**, 1236 (1994).
[240] G. Dollinger, M. Boulouednine, A. Bergmaier, T. Faestermann, and C. M. Frey, Nucl. Instrum. Methods Phys. Res. B **118**, 291 (1996).
[241] J. C. Barbour and B. L. Doyle, in *Handbook of Modern Ion Beam Materials Analysis*, edited by J. R. Tesmer and M. Nastasi (Materials Research Society, Pittsburgh, PA, 1995), pp. 83–138.
[242] B. Brijs, J. Deleu, T. Conard, H. D. Witte, W. Vandervorst, K. Nakajima, K. Kimura, I. Genchev, A. Bergmaier, L. Goergens, P. Neumaier, G. Dollinger, and M. Dobeli, Nucl. Instrum. Methods Phys. Res. B **161**, 429 (2000).
[243] H. T. Tang, W. N. Lennard, M. Zinke-Allmang, I. V. Mitchell, L. C. Feldman, M. L. Green, and D. Brasen, Appl. Phys. Lett. **64**, 64 (1994).
[244] W. N. Lennard, G. R. Massoumi, I. V. Mitchell, H. T. Tang, and D. F. Mitchell, Nucl. Instrum. Methods Phys. Res. B **85**, 42 (1994).
[245] I. J. R. Baumvol, F. C. Stedile, J. J. Ganem, I. Trimaille, and S. Rigo, Appl. Phys. Lett. **69**, 2385 (1996).
[246] I. J. R. Baumvol, J. J. Ganem, L. G. Gosset, I. Trimaille, and S. Rigo, Appl. Phys. Lett. **72**, 450 (1998).
[247] J. Rodriguez-Viejo, F. Sibieude, M. T. Clavaguera-Mora, and C. Monty, Appl. Phys. Lett. **63**, 1906 (1993).
[248] M. A. Douglas, S. Hattangady, and K. Eason, J. Electrochem. Soc. **147**, 1893 (2000).
[249] L. Meda, Physica B **170**, 259 (1991).
[250] A. Asano, Physica B **170**, 277 (1991).
[251] P. Asoka-Kumar, K. G. Lynn, T. C. Leung, B. Nielsen, G. W. Rubloff, and Z. A. Weinberg, Phys. Rev. B **44**, 5885 (1991).
[252] J. M. M. de Nijs and M. Clement, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 25.
[253] M. Clement, J. M. M. de Nijs, P. Balk, H. Schut, and A. van Veen, J. Appl. Phys. **81**, 1943 (1997).
[254] K. Yagi, Surf. Sci. Rep. **17**, 305 (1993).
[255] Z. L. Wang, Rep. Prog. Phys. **56**, 997 (1993).
[256] J. C. H. Spence, *Experimental High-Resolution Electron Microscopy* (Oxford University, New York, 1988).
[257] A. H. Carim and R. Sinclair, J. Electrochem. Soc. **134**, 741 (1987).
[258] A. H. Carim and A. Bhattacharyya, Appl. Phys. Lett. **46**, 872 (1985).
[259] S. C. Kao and R. H. Doremus, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 interface*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1993), p. 23.
[260] H. Fukuda, M. Yasuda, T. Iwabuchi, and S. Ohno, Appl. Surf. Sci. **60/61**, 359 (1992).
[261] P. E. Batson, Nature (London) **366**, 727 (1993).
[262] N. D. Browning, M. F. Chisholm, and S. J. Pennycook, Nature (London) **366**, 143 (1993).
[263] P. E. Batson, N. D. Browning, and D. A. Muller, Microsc. Soc. Amer. Bull. **24**, 371 (1994).
[264] J. M. Cowley, Surf. Rev. Lett. **4**, 567 (1997).
[265] G. Duscher, S. J. Pennycook, N. D. Browning, R. Rupangudi, C. Takoudis, H.-J. Gao, and R. Singh, in *Characterization and Metrology for ULSI Technology*, edited by D. G. Seiler, A. C. Diebold, W. M. Bullis, T. J. Shaffner, R. McDonald, and E. J. Walters (AIP, New York, 1998), Vol. 449, pp. 191–196.
[266] R. D. Twesten, J. M. Gibson, and F. M. Ross, MRS Bull. **29**, 38 (1994).
[267] F. M. Ross and J. M. Gibson, Phys. Rev. Lett. **68**, 1782 (1992).
[268] F. M. Ross, J. M. Gibson, and R. D. Twesten, Surf. Sci. **310**, 243 (1994).
[269] A. V. Latyshev, A. L. Aseev, A. B. Krasilnikov, and S. I. Stenin, Surf. Sci. **213**, 157 (1989).
[270] S. Fujita, H. Watanabe, S. Maruno, M. Ichikawa, and T. Kawamura, Appl. Phys. Lett. **71**, 885 (1997).
[271] H. Watanabe, K. Kato, T. Uda, K. Fujita, M. Ichikawa, T. Kawamura, and K. Terakura, Phys. Rev. Lett. **80**, 345 (1998).
[272] K. Wurm, R. Kliese, Y. Hong, B. Rottger, Y. Wei, H. Neddermeyer, and I. S. T. Tsong, Phys. Rev. B **50**, 1567 (1994).
[273] E. Bauer, Y. Wei, T. Müller, A. Pavlovska, and I. S. T. Tsong, Phys. Rev. B **51**, 17891 (1995).
[274] R. M. Tromp, A. W. Denier van der Gon, F. K. LeGoues, and M. C. Reuter, Phys. Rev. Lett. **71**, 3299 (1993).
[275] G. Binnig, H. Rohrer, C. Gerber, and E. Weibel, Appl. Phys. Lett. **40**, 178 (1982).
[276] G. Binnig, H. Rohrer, C. Gerber, and E. Weibel, Phys. Rev. Lett. **50**, 120 (1983).
[277] G. Binnig and H. Rohrer, IBM J. Res. Dev. **30**, 355 (1986).
[278] M. L. Lozano and M. C. Tringides, Europhys. Lett. **30**, 537 (1995).
[279] H. Neddermeyer, Rep. Prog. Phys. **59**, 701 (1996).
[280] M. Niwa, H. Iwasaki, Y. Watanabe, I. Sumita, N. Akutsu, and Y. Akutsu, Appl. Surf. Sci. **60/61**, 39 (1992).
[281] J. Seiple and J. P. Pelz, J. Vac. Sci. Technol. A **13**, 772 (1995).
[282] H. Neddermeyer, in *Surface Science: Principles and Applications*, edited by R. F. Howe, R. N. Lamb, and K. Wandelt (Springer-Verlag, Berlin, 1993).
[283] G. D. Wilk, Y. Wei, H. Edwards, and R. M. Wallace, Appl. Phys. Lett. **70**, 2288 (1997).
[284] F. M. Leibsle, A. Samsavar, and T. C. Chiang, Phys. Rev. B **38**, 5780 (1988).
[285] P. Avouris, I. W. Lyo, and F. Bozso, J. Vac. Sci. Technol. B **9**, 424 (1991).
[286] J. P. Pelz and R. H. Koch, J. Vac. Sci. Technol. B **9**, 775 (1991).
[287] P. Avouris and D. Cahill, Ultramicroscopy **42/44**, 838 (1992).
[288] R. Kliese, B. Rottger, D. Badt, and H. Neddermeyer, Ultramicroscopy **42/44A**, 824 (1992).
[289] J. Seiple, J. Pecquet, Z. Meng, and J. P. Pelz, J. Vac. Sci. Technol. A **11**, 1649 (1993).
[290] Y. Ono, M. Tabe, and H. Kageshima, Phys. Rev. B **48**, 14291 (1993).
[291] T. Hasegawa, M. Kohno, S. Hosaka, and S. Hosoki, Surf. Sci. **312**, L753 (1994).
[292] M. Udagawa, M. Niwa, and I. Sumita, Jpn. J. Appl. Phys., Part 1 **32**, 282 (1993).
[293] P. Avouris and R. J. Hamers, J. Vac. Sci. Technol. A **6**, 508 (1988).
[294] H. Neddermeyer, T. Doege, E. Harazim, R. Kliese, A. Kraus, R. Kulla, M. Mitte, and B. Rottger, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 277.
[295] R. M. Wallace and Y. Wei, J. Vac. Sci. Technol. B **17**, 970 (1999).
[296] Y. Morita and H. Tokumoto, Surf. Sci. Lett. **443**, L1037 (1999).
[297] A. G. Schrott, Q. X. Su, and S. C. Fain, Surf. Sci. **123**, 223 (1982).
[298] A. G. Schrott and S. C. Fain, Surf. Sci. **111**, 39 (1981).
[299] A. G. Schrott and S. C. Fain, Surf. Sci. **123**, 204 (1982).
[300] A. Feltz, U. Memmert, and R. J. Behm, Chem. Phys. Lett. **192**, 271 (1992).
[301] A. Feltz, U. Memmert, and R. J. Behm, Surf. Sci. **314**, 34 (1994).
[302] H. Watanabe, K. Fujita, and M. Ichikawa, Appl. Phys. Lett. **72**, 1987 (1998).
[303] J. E. Griffith and D. A. Grigg, J. Appl. Phys. **74**, R83 (1993).
[304] W. J. Kaiser and L. D. Bell, Phys. Rev. Lett. **60**, 1406 (1988).
[305] R. Ludeke and H. J. Wen, Microelectron. Eng. **36**, 255 (1997).
[306] C. Gao and X.-D. Xiang, Rev. Sci. Instrum. **69**, 3846 (1998).
[307] C. P. Vlahacos, R. C. Black, S. M. Anlage, A. Amar, and F. C. Wellstood, Appl. Phys. Lett. **69**, 3272 (1996).
[308] D. E. Steinhauer, C. P. Vlahacos, F. C. Wellstood, S. M. Anlage, C. Canedy, R. Ramesh, A. Stanishevsky, and J. Meingailis, Appl. Phys. Lett. **75**, 3180 (1999).
[309] D. E. Steinhauer, C. P. Vlahacos, F. C. Wellstood, S. M. Anlage, C. Canedy, R. Ramesh, A. Stanishevsky, and J. Meingailis, Rev. Sci. Instrum. **71**, 2751 (2000).
[310] Y. J. Huang, J. Slinkman, and C. C. Williams, Ultramicroscopy **42-44**, 298 (1992).
[311] P. Avouris, J. Phys. Chem. **94**, 2246 (1990).
[312] P. Avouris and I.-W. Lyo, Surf. Sci. **242**, 1 (1991).
[313] M. Mankos, R. M. Tromp, M. C. Reuter, and E. Cartier, Phys. Rev. Lett. **76**, 3200 (1996).
[314] Y. Huang, C. C. Williams, and J. Slinkman, Appl. Phys. Lett. **66**, 344 (1995).
[315] R. N. Kleiman, M. L. O'Malley, F. H. Baumann, J. P. Garno, and G. L. Timp, J. Vac. Sci. Technol. B **18**, 2034 (2000).
[316] E. H. Nicollian and J. R. Brews, *MOS Physics & Technology* (Wiley, New York, 1982).
[317] K. S. Krisch, J. Bude, and L. Manchanda, Electron Dev. Lett. **17**, 521 (1996).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[318] S.-H. Lo, D. A. Buchanan, and Y. Taur, IBM J. Res. Dev. **43**, 327 (1999).
[319] M. J. VanDort, P. H. Woerlee, and A. J. Walker, Solid-State Electron. **37**, 411 (1994).
[320] R. Rios and N. D. Arora, Tech. Dig. Int. Electron Devices Meet. **1994**, 613.
[321] C.-H. Choi, J.-S. Goo, T.-Y. Oh, Z. Yu, R. W. Dutton, A. Bayoumi, M. Cao, P. V. Voorde, D. Vook, and C. H. Diaz, IEEE Electron Device Lett. **20**, 292 (1999).
[322] R. Rios, N. D. Arora, and C.-L. Huang, IEEE Electron Device Lett. **15**, 129 (1994).
[323] W. K. Henson, K. Z. Ahmed, E. M. Vogel, J. R. Hauser, J. J. Wortman, R. D. Venables, M. Xu, and D. Venables, IEEE Electron Device Lett. **20**, 179 (1999).
[324] C.-H. Choi, J.-S. Goo, T.-Y. Oh, Z. Yu, R. Dutton, A. Bayoumi, M. Cao, P. V. Voorde, and D. Vook, VLSI Tech. Dig. **1999**, 63.
[325] R. H. Fowler and L. Nordheim, Proc. R. Soc. London, Ser. A **119**, 173 (1928).
[326] D. J. DiMaria and M. V. Fischetti, Appl. Surf. Sci. **30**, 278 (1987).
[327] K. F. Schuegraf and C. Hu, VLSI Tech. Dig. **1992**, 18.
[328] L. Lai and E. A. Irene, J. Appl. Phys. **87**, 1159 (2000).
[329] M. Depas, B. Vermeire, P. W. Mertens, R. L. V. Meirhaeghe, and M. M. Heyns, Solid-State Electron. **38**, 1465 (1995).
[330] K. F. Schuegraf and C. Hu, IEEE Trans. Electron Devices **41**, 761 (1994).
[331] W.-C. Lee and C. Hu, VLSI Tech. Dig. **2000**, 198.
[332] Khairurrijal, W. Mizubayashi, S. Miyazaki, and M. Hirose, J. Appl. Phys. **87**, 3000 (2000).
[333] L. F. Register, E. Rosenbaum, and K. Yang, Appl. Phys. Lett. **74**, 457 (1999).
[334] V. E. Houtsma, J. Holleman, C. Salm, F. P. Widdershoven, and P. H. Woerlee, IEEE Electron Device Lett. **20**, 314 (1999).
[335] C. Salm, J. H. Klootwijk, Y. Ponomarev, P. W. H. Boos, D. J. Gravesteijn, and P. H. Woerlee, IEEE Electron Device Lett. **19**, 213 (1998).
[336] J. L. Ogier, R. Degraeve, P. Roussel, G. Groeseneken, and H. E. Maes, Proc. of the 26th Eur. Sol. State Dev. Res. Conf. (1996), pp. 763–766.
[337] W.-C. Lee, T.-J. King, and C. Hu, IEEE Electron Device Lett. **20**, 268 (1999).
[338] G. Groeseneken, H. E. Maes, N. Beltràn, and R. F. D. Keersmaecker, IEEE Trans. Electron Devices **31**, 42 (1984).
[339] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, IEEE Trans. Electron Devices **36**, 1318 (1989).
[340] P. Masson, J.-L. Autran, and J. Brini, IEEE Electron Device Lett. **20**, 92 (1999).
[341] D. J. DiMaria, E. Cartier, and D. Arnold, J. Appl. Phys. **73**, 3367 (1993).
[342] D. J. DiMaria, D. A. Buchanan, J. H. Stathis, and R. E. Stahlbush, J. Appl. Phys. **77**, 2032 (1995).
[343] A. Ghetti, E. Sangiorgi, J. Bude, T. W. Sorsch, and G. Weber, Tech. Dig. Int. Electron Devices Meet. **1999**, 731.
[344] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, Tech. Dig. Int. Electron Devices Meet. **1995**, 863.
[345] R. Degraeve, G. Groeseneken, R. Bellens, J. L. Ogier, M. Depas, P. Roussel, and H. E. Maes, IEEE Trans. Electron Devices **45**, 904 (1998).
[346] D. J. DiMaria, D. Arnold, and E. Cartier, Appl. Phys. Lett. **60**, 2118 (1992).
[347] T. Nigam, R. Degraeve, G. Groeseneken, M. M. Heyns, and H. E. Maes, Proc. IRPS , 381 (1999).
[348] I. C. Chen, S. Holland, and C. Hu, Proc. IRPS , 24 (1985).
[349] I. C. Chen, S. Holland, K. K. Young, C. Chang, and C. Hu, Appl. Phys. Lett. **49**, 669 (1986).
[350] C. Monsérié, C. Papadas, G. Ghibaudo, C. Gounelle, P. Mortini, and G. Pananakakis, Proc. IRPS , 280 (1993).
[351] E. Vincent, C. Papadas, C. Riva, F. Pio, and G. Ghibaudo, Proc. of the 26th Eur. Sol. State Dev. Res. Conf. (1994), pp. 495–498.
[352] E. Vincent, C. Papadas, and G. Ghibaudo, Proc. of the 26th Eur. Sol. State Dev. Res. Conf. (1996), pp. 767–770.
[353] Z. A. Weinberg and M. V. Fischetti, J. Appl. Phys. **59**, 824 (1986).
[354] I. C. Chen, S. Holland, and C. Hu, IEEE Electron Device Lett. **7**, 164 (1986).
[355] D. J. DiMaria, IEEE Electron Device Lett. **16**, 184 (1995).
[356] K. F. Schuegraf and C. Hu, J. Appl. Phys. **76**, 3695 (1994).
[357] M. V. Fischetti, Phys. Rev. B **31**, 2099 (1985).
[358] D. J. DiMaria, E. Cartier, and D. A. Buchanan, J. Appl. Phys. **80**, 304 (1996).
[359] M. Rasras, I. D. Wol, G. Groeseneken, B. Kaczer, R. Degraeve, and H. E. Maes, Tech. Dig. Int. Electron Devices Meet. **1999**, 465.
[360] H. Satake and A. Toriumi, Tech. Dig. Int. Electron Devices Meet. **1993**, 337.
[361] R. Degraeve, J. L. Ogier, R. Bellens, P. Roussel, G. Groeseneken, and H. E. Maes, IEEE Trans. Electron Devices **45**, 472 (1998).
[362] A. Teramoto, K. Kabayashi, Y. Matsui, M. Hirayama, and A. Yasuoka, Proc. IRPS , 113 (1996).
[363] M. F. Li, Y. D. He, S. G. Ma, B.-J. Cho, K. F. Lo, and M. Z. Xu, IEEE Electron Device Lett. **20**, 586 (1999).
[364] B. Kaczer, R. Degraeve, N. Pangon, and G. Groeseneken, IEEE Trans. Electron Devices **47**, 1514 (2000).
[365] D. J. Dumin, J. R. Maddux, R. S. Scott, and R. Subramoniam, IEEE Trans. Electron Devices **41**, 1570 (1994).
[366] E. F. Runnion, S. M. G. IV, R. S. Scott, D. J. Dumin, L. Lie, and J. Mitros, Proc. IRPS , 93 (1996).
[367] T. H. Ning, Solid-State Electron. **21**, 273 (1978).
[368] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, J. Appl. Phys. **60**, 2024 (1986).
[369] R. Degraeve, G. Groeseneken, I. D. Wolf, and H. E. Maes, Microelectron. Eng. **28**, 313 (1995).
[370] A. Modelli and B. Ricco, Tech. Dig. Int. Electron Devices Meet. **1984**, 148.
[371] P. P. Apte and K. C. Saraswat, Proc. IRPS , 136 (1994).
[372] E. Avni and J. Shappir, J. Appl. Phys. **64**, 743 (1988).
[373] J. Suñé, I. Placencia, N. Barniol, E. Farrés, F. Martín, and X. Aymerich, Thin Solid Films **185**, 347 (1990).
[374] K. R. Farmer, R. Saletti, and R. A. Buhrman, Appl. Phys. Lett. **52**, 1749 (1988).
[375] P. Olivo, T. N. Nguyen, and B. Ricco, IEEE Trans. Electron Devices **35**, 2259 (1988).
[376] N. K. Patel and A. Toriumi, Appl. Phys. Lett. **64**, 1809 (1994).
[377] J. DeBlauwe, J. V. Houdt, D. Wellekens, R. Degraeve, P. Roussel, L. Haspeslagh, L. Deferm, G. Groeseneken, and H. E. Maes, Tech. Dig. Int. Electron Devices Meet. **1996**, 343.
[378] R. Moazzami and C. Hu, Tech. Dig. Int. Electron Devices Meet. **1992**, 139.
[379] J. DeBlauwe, R. Degraeve, R. Bellens, J. V. Houdt, P. Roussel, G. Groeseneken, and H. E. Maes, Proc. of the 26th Eur. Sol. State Dev. Res. Conf. (1996), pp. 361–364.
[380] M. Kato, N. Myamoto, H. Hume, A. Satoh, T. Adachi, M. Ushiyama, and K. Kimura, Tech. Dig. Int. Electron Devices Meet. **1994**, 45.
[381] N.-K. Zous, T. Wang, C.-C. Yeh, and C. W. Tsai, Appl. Phys. Lett. **75**, 734 (1999).
[382] T. Wang, N.-K. Zous, J.-L. Lai, and C. Huang, IEEE Electron Device Lett. **19**, 148 (1998).
[383] P. Riess, G. Ghibaudo, and G. Pananakakis, Appl. Phys. Lett. **75**, 3871 (1999).
[384] B. Ricco, G. Gozzi, and M. Lanzoni, IEEE Trans. Electron Devices **45**, 1554 (1998).
[385] J. Wu, L. F. Register, and E. Rosenbaum, Proc. IRPS , 389 (1999).
[386] P. E. Nicollian, M. Rodder, D. T. Grider, P. Chen, R. M. Wallace, and S. V. Hattangady, Proc. IRPS , 400 (1999).
[387] H. Satake and A. Toriumi, Appl. Phys. Lett. **67**, 3489 (1995).
[388] P. Riess, G. Ghibaudo, and G. Pananakakis, J. Appl. Phys. **87**, 4626 (2000).
[389] K. Okada, H. Kubo, A. Ishinaga, and K. Yoneda, VLSI Proc. **1998**, 158.
[390] K. Okada, Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials (1997), p. 92.
[391] A. Ghetti, J. Bude, and G. Weber, IEEE Trans. Elec. Dev. **48**, 1354 (2001).
[392] I. C. Chen, S. Holland, and C. Hu, J. Appl. Phys. **61**, 4544 (1987).
[393] H. Uchida and T. Ajika, Appl. Phys. Lett. **51**, 433 (1987).
[394] H. Satake, S. Takagi, and A. Toriumi, Proc. IRPS , 156 (1997).
[395] C.-L. Chiang and N. Khurana, Tech. Dig. Int. Electron Devices Meet. **1986**, 672.
[396] E. Cartier, J. S. Tsang, M. V. Fischetti, and D. A. Buchanan, Microelectron. Eng. **36**, 103 (1997).
[397] J. D. Bude, B. E. Weir, and P. J. Silverman, Tech. Dig. Int. Electron Devices Meet. **1998**, 179.
[398] M. A. Alam, J. Bude, and A. Ghetti, Proc. IRPS, 21 (2000).
[399] R. S. Scott, N. A. Dumin, T. W. Hughes, D. J. Dumin, and B. T. Moore, Proc. IRPS, 131 (1995).
[400] J. W. McPherson and D. A. Baglee, Proc. IRPS, 1 (1985).
[401] B. Schlund, C. Messick, J. S. Suehle, and P. Chaparala, Proc. IRPS, 84 (1996).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[402] J. W. McPherson and H. C. Mogul, Proc. IRPS, 47 (1998).
[403] M. Kimura, IEEE Trans. Electron Devices **46**, 220 (1999).
[404] D. J. DiMaria, J. Appl. Phys. **65**, 2342 (1989).
[405] E. Cartier and J. H. Stathis, Microelectron. Eng. **28**, 3 (1995).
[406] J. Wu, E. Rosenbaum, B. MacDonald, E. Li, J. Tao, B. Tracy, and P. Fang, IRPS Proc., 27 (2000).
[407] Y. Mitani, H. Satake, H. Ito, and A. Toriumi, Tech. Dig. Int. Electron Devices Meet. **2000**, 343.
[408] Y. Mitani, H. Satake, H. Ito, and A. Toriumi, Jpn. J. Appl. Phys., Part 2 **39**, L564 (2000).
[409] R. Subramoniam, R. S. Scott, and D. J. Dumin, Tech. Dig. Int. Electron Devices Meet. **1992**, 135.
[410] N. Shiono and M. Itsumi, Proc. IRPS, 1 (1993).
[411] B. I. Shklosskii and A. L. Efros, *Electronic Properties of Doped Semiconductors* (Springler-Verlag, Berlin, 1984).
[412] H. Z. Massoud and R. Deaton, Extended Abstracts of the Electrochem. Soc. Meeting (ECS, Pennington, NJ, 1994), p. 287.
[413] G. M. Paulzen, Microelectron. Eng. **36**, 321 (1997).
[414] D. R. Wolters and J. F. Verweij, *Insulating Films on Semiconductors* (Elsevier, Amsterdam, 1986), pp. 332–335.
[415] T. Nigam, R. Degraeve, G. Groeseneken, M. M. Heyns, and H. E. Maes, Proc. IRPS, 62 (1998).
[416] K. Okada, S. Kawasaki, and Y. Hirofuji, Extended Abstracts of the 1994 International Conference on Sol. State Devices and Materials (1994), p. 565.
[417] S. H. Lee, B. J. Cho, J. C. Kim, and S. H. Choi, Tech. Dig. Int. Electron Devices Meet. **1994**, 605.
[418] M. Depas, T. Nigam, and M. Heyns, IEEE Trans. Electron Devices **43**, 1499 (1996).
[419] K. Okada and K. Taniguchi, Appl. Phys. Lett. **70**, 351 (1997).
[420] K. P. Cheung, J. I. Colonell, C. P. Chang, W. Y. C. Lai, C. T. Liu, R. Liu, and C. S. Pai, Symp. VLSI Technol. Dig. **1997**, 145.
[421] F. Crupi, R. Degraeve, G. Groeseneken, T. Nigam, and H. E. Maes, IEEE Trans. Electron Devices **45**, 2329 (1998).
[422] C. Leroux, D. Blachier, O. Briere, and G. Reimbold, Microelectron. Eng. **36**, 297 (1997).
[423] O. Briere, J. A. Chroboczek, and G. Ghibaudo, Proc. of the 26th Eur. Sol. State Dev. Res. Conf. (1996), p. 759.
[424] A. Ohata, A. Toriumi, M. Iwase, and K. Natori, J. Appl. Phys. **68**, 200 (1990).
[425] E. Wu, E. Nowak, J. Aitken, W. Abadeer, L. K. Han, and S. Lo, Tech. Dig. Int. Electron Devices Meet. **1998**, 187.
[426] T. Pompl, H. Wurzer, M. Kerber, R. C. W. Wilkins, and I. Eisele, Proc. IRPS, 82 (1999).
[427] T. Sakura, H. Utsunomiya, Y. Kamakura, and K. Taniguchi, Tech. Dig. Int. Electron Devices Meet. **1998**, 183.
[428] M. A. Alam, B. Weir, J. Bude, P. Silverman, and D. Monroe, Tech. Dig. Int. Electron Devices Meet. **1999**, 449.
[429] R. Degraeve, B. Kaczer, and G. Groeseneken, Semicond. Sci. Technol. **15**, 436 (2000).
[430] E. Y. Wu, J. H. Stathis, and L.-K. Han, Semicond. Sci. Technol. **15**, 425 (2000).
[431] S. Bruyere, E. Vincent, and G. Ghibaudo, Proc. of the 26th Eur. Sol. State Dev. Res. Conf. (2000), p. 48.
[432] N. Vandewalle, M. Ausloos, M. Houssa, P. W. Mertens, and M. M. Heyns, Appl. Phys. Lett. **74**, 1579 (1999).
[433] E. Miranda, J. Suñé, R. Rodríguez, M. Nafría, and X. Aymerich, Proc. IRPS, 42 (1998).
[434] J. Suñé, E. Miranda, M. Nafría, and X. Aymerich, Appl. Phys. Lett. **75**, 959 (1999).
[435] J. Suñé, E. Miranda, M. Nafría, and X. Aymerich, Tech. Dig. Int. Electron Devices Meet. **1998**, 191.
[436] M. Nafría, J. Suñé, and X. Aymerich, J. Appl. Phys. **73**, 205 (1993).
[437] G. B. Alers, B. E. Weir, M. A. Alam, G. L. Timp, and T. Sorsch, Proc. IRPS, 76 (1998).
[438] Y. D. He, G. H. M. F. Li, B. J. Cho, and Z. Dong, Appl. Phys. Lett. **75**, 2432 (1999).
[439] B. E. Weir, P. J. Silverman, M. A. Alam, F. Baumann, D. Monroe, A. Ghetti, J. D. Bude, G. L. Timp, A. Hamad, T. M. Oberdick, N. X. Zhao, Y. Ma, M. M. Brown, D. Hwang, T. W. Sorsch, and J. Madic, Tech. Dig. Int. Electron Devices Meet. **1999**, 437.
[440] R. Degraeve, B. Kaczer, A. DeKeersgieter, and G. Groeseneken, Proc. IEEE Int. Reliability Phys. Sym. (2001), p. 360.
[441] B. Linder, J. H. Stathis, R. A. Wachnik, E. Wu, S. A. Cohen, A. Ray, and A. Vayshenker, VLSI Tech. Dig., 214 (2000).
[442] B. E. Weir, M. A. Alam, and P. J. Silverman, Microelectron. Eng. (in press).
[443] R. Degraeve, N. Pangon, B. Kaczer, T. Nigam, G. Groeseneken, and A. Naem, Symposium on VLSI Tech. Dig., 59 (1999).
[444] J. S. Suehle, P. Chaparala, C. Messick, W. M. Miller, and K. C. Boyko, in *Field and Temperature Acceleration of Time-Dependent Dielectric Breakdown in Intrinsic Thin SiO2* (1994), pp. 120–125.
[445] K. F. Schuegraf and C. Hu, Semicond. Sci. Technol. **9**, 989 (1994).
[446] A. Yassine, H. E. Nariman, and K. Olasupo, IEEE Electron Device Lett. **20**, 390 (1999).
[447] P. E. Nicollian, W. R. Hunter, and J. C. Hu, Proc. IRPS, 7 (2000).
[448] J. M. McKenna, E. Y. Wu, and S.-H. Lo, Proc. IRPS, 16 (2000).
[449] R. P. Vollertsen, ESREF, 97 (1992).
[450] K. Okada and K. Yoneda, Tech. Dig. Int. Electron Devices Meet. **1999**, 445.
[451] K. P. Cheung, Tech. Dig. Int. Electron Devices Meet. (1999).
[452] C. Hu and Q. Lu, Proc. IRPS, 47 (1999).
[453] D. J. DiMaria, J. Appl. Phys. **81**, 3220 (1997).
[454] C.-C. Chen, C.-Y. Chang, C.-H. Chien, T.-H. Huang, H.-C. Lin, and M.-S. Liang, Appl. Phys. Lett. **74**, 3708 (1999).
[455] O. Brière, A. Halimaoui, and G. Ghibaudo, Solid-State Electron. **41**, 981 (1997).
[456] A. Teramoto, H. Umeda, K. Azamawari, K. Kobayashi, K. Shiga, J. Komori, Y. Ohno, and H. Miyoshi, Proc. IRPS, 66 (1999).
[457] B. Kaczer, R. Degraeve, N. Pangon, T. Nigam, and G. Groeseneken, Microelectron. Eng. **48**, 47 (1999).
[458] D. J. DiMaria and J. H. Stathis, Appl. Phys. Lett. **74**, 1752 (1999).
[459] J. H. Stathis, A. Vayshenker, P. R. Varakamp, C. M. E. Y. Wu, J. McKenna, D. J. DiMaria, L.-K. Han, E. Cartier, R. A. Wachnik, and B. P. Linder, Symposium on VLSI Tech. Dig., 94 (2000).
[460] P. Singer, Semicond. Int. October, 88 (1995).
[461] T. Couteau, M. McBride, D. Riley, and P. Peavey, Semicond. Int. **21**, 95 (1998).
[462] T. Hattori, Solid State Technol. **38**, 7 (1995).
[463] M. M. Heyns, IBM J. Res. Dev. **43**, 339 (1999).
[464] W. Kern, J. Electrochem. Soc. **137**, 1887 (1990).
[465] *Chemical Surface Preparation, Passivation and Cleaning for Semiconductor Growth and Processing*, edited by R. J. Nemanich, C. R. Helms, M. Hirose, and G. W. Rubloff (Materials Research Society, Pittsburgh, 1992), Vol. 259.
[466] T. Ohmi, J. Electrochem. Soc. **143**, 2957 (1996).
[467] H. F. Okorn-Schmidt, IBM J. Res. Dev. **43**, 351 (1999).
[468] G. S. Higashi and Y. J. Chabal, in *Handbook of Silicon Wafer Cleaning Technology*, edited by W. Kern (Noyes, Park Ridge, NJ, 1993), p. 433.
[469] J. Sapjeta, T. Boone, J. M. Rosamilia, P. J. Silverman, T. W. Sorsch, G. Timp, and B. E. Weir, in *Science and Technology of Semiconductor Surface Preparation*, edited by M. H. G. Higashi, S. Raghavan, and S. Verhaverbeke (Materials Research Society, Pittsburgh, 1997), Vol. 477, pp. 203–208.
[470] M. Miyashita, T. Tusga, K. Makihara, and T. Ohmi, J. Electrochem. Soc. **139**, 2133 (1992).
[471] C. H. Bjorkman, T. Yasuda, J. C. E. Shearson, Y. Ma, G. Lucovsky, U. Emmerichs, C. Meyer, K. Leo, and H. Kurz, J. Vac. Sci. Technol. B **11**, 1521 (1993).
[472] H. Morinaga, M. Suyama, and T. Ohmi, J. Electrochem. Soc. **141**, 2834 (1994).
[473] T. Ohmi, T. Imaoka, I. Sugiyama, and T. Kezuka, J. Electrochem. Soc. **139**, 3317 (1992).
[474] S. R. Kasi, M. Liehr, P. A. Thiry, H. Dallaporta, and M. Offenberg, Appl. Phys. Lett. **59**, 108 (1991).
[475] Y. Sugita, S. Watanabe, and N. Awaji, Jpn. J. Appl. Phys., Part 1 **35**, 5437 (1996).
[476] R. Iscoff, Semicond. Int. **16**, 58 (1993).
[477] Y. Ma, M. L. Green, L. C. Feldman, J. Sapjeta, K. J. Hanson, and T. W. Weidman, J. Vac. Sci. Technol. B **13**, 1460 (1995).
[478] K. Torek, J. Ruzyllo, R. Grant, and R. Novak, J. Electrochem. Soc. **142**, 1322 (1995).
[479] H. Park, D. Ko, P. Apte, C. R. Helms, and K. C. Saraswat, Electrochem. Solid-State Lett. **1**, 77 (1998).
[480] J. Ruzyllo, E. Rohr, M. Baeyens, T. Bearda, P. Mertens, and M. Heyns, in *Gas-Phase Surface Processing Prior to 3.2 nm Gate Oxidation* (Ostend, Belgium, 1998).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[481] Y. Ma, M. L. Green, K. Torek, J. Ruzyllo, R. Opila, K. Konstandinidis, D. Siconolfi, and D. Brasen, J. Electrochem. Soc. **142**, L217 (1995).
[482] T. Sorsch, W. Timp, F. H. Baumann, K. H. A. Bogart, T. Boone, V. M. Donnelly, M. L. Green, K. Evans-Lutterodt, C. Y. Kim, S. Moccio, J. Rosamilia, J. Sapjeta, P. Silverman, B. Weir, and G. Timp, VLSI Tech. Dig., 222 (1998).
[483] B. E. Deal and A. S. Grove, J. Appl. Phys. **36**, 3770 (1965).
[484] S. Bruyere, F. Guyader, W. D. Coster, E. Vincent, M. Saadeddine, N. Revil, and G. Ghibaudo, Microelectron. Reliab. **40**, 691 (2000).
[485] Y. Murakami, T. Shiota, T. Shingyouji, and H. Abe, J. Appl. Phys. **75**, 5302 (1994).
[486] R. R. Razouk and B. E. Deal, J. Electrochem. Soc. **126**, 1573 (1979).
[487] K. H. Lee, W. H. Liu, S. A. Campbell, and I. Banerjee, J. Electrochem. Soc. **140**, 501 (1993).
[488] C. Hashimoto, S. Muramoto, N. Shiomo, and O. Nakajima, J. Electrochem. Soc. **127**, 129 (1980).
[489] E. A. Taft, J. Electrochem. Soc. **125**, 968 (1978).
[490] S. V. Hattangady, H. Niimi, and G. Lucovsky, J. Vac. Sci. Technol. A **14**, 3017 (1996).
[491] Y. Ma, T. Yasuda, and G. Lucovsky, Appl. Phys. Lett. **64**, 2226 (1994).
[492] J. D. Plummer, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface-3*, edited by H. Z. Massoud, E. H. Poindexter, and C. R. Helms (Electrochemical Society, Pennington, NJ, 1996).
[493] B. E. Deal, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1988), p. 5.
[494] E. P. Gusev, H. C. Lu, T. Gustafsson, and E. Garfunkel, in *Interface Control of Electrical, Chemical, and Mechanical Properties*, edited by S. P. Murarka, K. Rose, T. Ohmi, and T. Seidel (Materials Research Society, Pittsburgh, 1994), Vol. 318, p. 69.
[495] A. M. Stoneham, C. R. M. Grovenor, and A. Cerezo, Philos. Mag. B **55**, 201 (1987).
[496] S. Matsushita, Semicond. Int. **20**, 339 (1997).
[497] A. Dip, Solid State Technol. **39**, 113 (1996).
[498] V. Khemka and T. P. Chow, J. Electrochem. Soc. **144**, 1137 (1997).
[499] Z. Cui, J. M. Madsen, and C. G. Takoudis, J. Appl. Phys. **87**, 8181 (2000).
[500] A. Kurokawa, T. Maeda, K. Sakamoto, H. Itoh, K. Nakamura, K. Koike, D. W. Moon, Y. H. Ha, S. Ichimura, and A. Ando, in *Ultrathin SiO2 Formation by O3 on Ultraflat Si Surface* (Materials Research Society, San Francisco, 1999), pp. 21–26.
[501] K. Koike, G. Inoue, S. Ichimura, K. Nakamura, A. Kurokawa, and H. Nonaka, in *Development of High Purity One ATM Ozone Source—It's Application to Ultrathin SiO2 Film Formation on Si Substrate* (Materials Research Society, San Francisco, 1999), pp. 121–126.
[502] A. Kazor, R. Gwilliam, and I. W. Boyd, Appl. Phys. Lett. **65**, 412 (1994).
[503] A. Kazor and I. W. Boyd, Appl. Phys. Lett. **63**, 2517 (1993).
[504] Y. Yu and G. Lucovsky, IEEE Electron Device Lett. **EDL-19**, 367 (1998).
[505] H. Niimi and G. Lucovsky, J. Vac. Sci. Technol. B **17**, 2610 (1999).
[506] G. Lucovsky, IBM J. Res. Dev. **43**, 301 (1999).
[507] R. Moazzami and C. Hu, IEEE Electron Device Lett. **14**, 72 (1993).
[508] P. K. McLarty, W. L. Hill, X.-L. Xu, V. Misra, J. J. Wortman, and G. S. Harris, Appl. Phys. Lett. **63**, 3619 (1993).
[509] M. Liehr and S. A. Cohen, Appl. Phys. Lett. **60**, 198 (1992).
[510] H.-H. Tseng and P. J. Tobin, Semicond. Int. **15**, 68 (1992).
[511] W. Gasser, Y. Uchida, and M. Matsumura, Thin Solid Films **250**, 213 (1994).
[512] S. M. George, O. Sneh, and J. D. Way, Appl. Surf. Sci. **82/83**, 460 (1994).
[513] D. Wang, T.-P. Ma, J. W. Golz, B. L. Halpern, and J. J. Schmitt, IEEE Electron Device Lett. **13**, 482 (1992).
[514] X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, B. L. Halpern, and J. J. Schmitt, VLSI Tech. Dig., 49 (1995).
[515] H.-H. Tseng, P. G. Y. Tsui, P. J. Tobin, J. Mogab, M. Khare, X. W. Wang, T. P. Ma, R. Hegde, C. Hobbs, J. Veteran, M. Hartig, G. Kenig, V. Wang, R. Blumenthal, R. Cotton, V. Kaushik, T. Tamagawa, B. L. Halpern, G. J. Cui, and J. J. Schmitt, Tech. Dig. Int. Electron Devices Meet. **1997**, 647.
[516] W. Kern and D. A. Puotinen, RCA Rev. **31**, 187 (1970).
[517] F. DeSmedt, C. Vinckier, I. Cornelissen, S. DeGendt, and M. Heyns, J. Electrochem. Soc. **147**, 1124 (2000).
[518] H. R. Soleimani, B. S. Doyle, and A. Philipossian, J. Electrochem. Soc. **142**, L132 (1995).
[519] C. T. Liu, E. J. Lloyd, Y. Ma, M. Du, R. L. Opila, and S. J. Hillenius, Tech. Dig. Int. Electron Devices Meet. **1996**, 499
[520] R. Hezel and N. Lieske, J. Electrochem. Soc. **129**, 379 (1982).
[521] M. L. Green, D. Brasen, L. C. Feldman, W. Lennard, and H. T. Tang, Appl. Phys. Lett. **67**, 1600 (1995).
[522] C. Lin, A. I. Chou, P. Choudhury, J. C. Lee, K. Kumar, B. Doyle, and H. R. Soleimani, Appl. Phys. Lett. **69**, 3701 (1996).
[523] J. A. Diniz, P. J. Tatsch, and M. A. A. Pudenzi, Appl. Phys. Lett. **69**, 2214 (1996).
[524] I. J. R. Baumvol, C. Krug, F. C. Stedile, M. L. Green, D. C. Jacobson, D. Eaglesham, J. D. Bernstein, J. Shao, A. S. Denholm, and P. L. Kellerman, Appl. Phys. Lett. **74**, 806 (1999).
[525] R. Kraft, T. P. Schneider, W. W. Dostalik, and S. Hattangady, J. Vac. Sci. Technol. B **15**, 967 (1997).
[526] D. T. Grider, S. V. Hattangaddy, R. Kraft, P. E. Nicollian, J. Kuehne, G. Brown, S. Aur, R. H. Eklund, M. F. Pas, W. R. Hunter, and M. Douglas, VLSI Tech. Dig., 47 (1997).
[527] S. V. Hattangady, R. Kraft, D. T. Grider, G. A. Brown, P. A. Tiner, J. W. Kuehne, P. E. Nicollian, and M. F. Pas, Tech. Dig. Int. Electron Devices Meet. **1996**, 495.
[528] K. Sekine, Y. Saito, M. Hirayama, and T. Ohmi, J. Vac. Sci. Technol. A **17**, 3129 (1999).
[529] Y. Saito, Appl. Phys. Lett. **68**, 800 (1996).
[530] H. Ohta, A. Nagashima, M. Ito, M. Hori, and T. Goto, J. Vac. Sci. Technol. B **18**, 2486 (2000).
[531] H. Nakamura, M. Kaneko, S. Matsumoto, S. Fujita, and A. Sasaki, Appl. Phys. Lett. **43**, 691 (1983).
[532] T. Mizokuro, K. Yoneda, Y. Todokoro, and H. Kobayashi, J. Appl. Phys. **85**, 2921 (1999).
[533] S. A. Bell, and D. W. Hess, J. Electrochem. Soc. **139**, 2904 (1992).
[534] C. T. Gabriel, Semicond. Int. July, 151 (1997).
[535] Y. Z. Hu, M. Li, Y. Wang, E. A. Irene, M. C. Hugon, F. Varniere, N. Jiang, M. Froment, and B. Agius, J. Vac. Sci. Technol. B **13**, 227 (1995).
[536] M. Revitz, S. I. Raider, and R. A. Gdula, J. Vac. Sci. Technol. **16**, 345 (1979).
[537] G. Lucovsky, A. Banerjee, B. Hinds, B. Claflin, K. Koh, and H. Yang, Microelectron. Eng. **36**, 207 (1997).
[538] K. Taniguchi, M. Tanaka, C. Hamaguchi, and K. Imai, J. Appl. Phys. **67**, 2195 (1990).
[539] B. J. Mrstik, V. V. Afanas'ev, A. Stesmans, P. J. McMarr, and R. K. Lawrence, J. Appl. Phys. **85**, 6577 (1999).
[540] X. Chen and J. M. Gibson, J. Electrochem. Soc. **146**, 3032 (1999).
[541] A. Ogura, J. Electrochem. Soc. **138**, 807 (1991).
[542] A. Stesmans and V. V. Afanas'ev, Phys. Rev. B **54**, R11 129 (1996).
[543] J. F. Conley and P. M. Lenahan, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface-3; Vol. 96-1*, edited by H. Z. Massoud, E. H. Poindexter, and C. R. Helms (Electrochemical Society, Pennington, NJ, 1996), p. 214.
[544] E. H. Poindexter, G. J. Gerardi, and D. J. Keeble, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface-3*, edited by H. Z. Massoud, E. H. Poindexter, and C. R. Helms (Electrochemical Society, Pennington, NJ, 1996), p. 172.
[545] R. H. Doremus, J. Phys. Chem. **80**, 1773 (1976).
[546] R. E. Stahlbush, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface-3*, edited by H. Z. Massoud, E. H. Poindexter, and C. R. Helms (Electrochemical Society, Pennington, NJ, 1996), p. 525.
[547] E. H. Poindexter, C. F. Young, and G. J. Gerardi, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. P. G. E. Garfunkel and A. Vul' (Kluwer, Dordrecht, 1998), p. 397.
[548] D. A. Buchanan, D. J. DiMaria, C.-A. Chang, and Y. Taur, Appl. Phys. Lett. **65**, 1820 (1994).
[549] E. Cartier, D. A. Buchanan, J. H. Stathis, and D. J. DiMaria, J. Non-Cryst. Solids **187**, 244 (1995).
[550] K. L. Brower, Phys. Rev. B **42**, 3444 (1990).
[551] P. M. Lenahan, Appl. Phys. Lett. **71**, 3126 (1997).
[552] R. H. Doremus, *Glass Science* (Wiley, New York, 1973).
[553] J. E. Shelby, J. Appl. Phys. **48**, 3387 (1977).
[554] D. L. Griscom, J. Appl. Phys. **58**, 2524 (1985).
[555] R. Gale, H. Chew, F. J. Feigl, and C. W. Magee, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1988), p. 177.
[556] M. A. George, D. A. Bohling, J. J. Wortman, J. A. Melzak, and G. A. Hames, J. Vac. Sci. Technol. B **11**, 86 (1993).
[557] J. Krauser, A. Weidinger, and D. Braunig, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface-3*, edited by H. Z. Massoud, E. H. Poindexter, and C. R. Helms (Electrochemical Society, Pennington, NJ, 1996), p. 184.

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[558] E. Cartier, D. A. Buchanan, and G. J. Dunn, Appl. Phys. Lett. **64**, 901 (1994).
[559] J. H. Stathis and E. Cartier, Phys. Rev. Lett. **72**, 2745 (1994).
[560] E. Cartier, J. H. Stathis, and D. A. Buchanan, Appl. Phys. Lett. **63**, 1510 (1993).
[561] P. E. Bloechl and J. Stathis, Physica B **273/4**, 1022 (1999).
[562] S. M. Myers, J. Appl. Phys. **61**, 5428 (1987).
[563] Q. Qiu, E. Arai, and Y. Ohji, Nucl. Instrum. Methods Phys. Res. B **56/57**, 816 (1991).
[564] H. Park and C. R. Helms, J. Electrochem. Soc. **139**, 2042 (1992).
[565] H. Fukuda, T. Ueno, H. Kawarada, and I. Ohdomari, Jpn. J. Appl. Phys., Part 2 **32**, L569 (1993).
[566] N. S. Saks and R. W. Rendell, IEEE Trans. Nucl. Sci. **39**, 2220 (1992).
[567] J. M. Lyding, K. Hess, and I. C. Kizilyalli, Appl. Phys. Lett. **68**, 2526 (1996).
[568] R. A. B. Devine, J.-L. Autran, W. L. Warren, K. L. Vanheusdan, and J.-C. Rostaing, Appl. Phys. Lett. **70**, 2999 (1997).
[569] H. C. Mogul, L. Cong, R. M. Wallace, P. J. Chen, T. A. Rost, and K. Harvey, Appl. Phys. Lett. **72**, 1721 (1998).
[570] R. Biswas, Y. P. Li, and B. C. Pan, Appl. Phys. Lett. **72**, 3500 (1998).
[571] K. Hess, I. C. Kizilyalli, and J. W. Lyding, IEEE Trans. Electron Devices **45**, 406 (1998).
[572] W. F. Clark, T. G. Ference, T. B. Hook, K. M. Watson, S. W. Mittl, and J. S. Burnham, IEEE Electron Device Lett. **20**, 48 (1999).
[573] T. G. Ference, J. S. Burnham, W. F. Clark, T. B. Hook, S. W. Mittl, K. M. Watson, and L.-K. K. Han, IEEE Trans. Electron Devices **46**, 747 (1999).
[574] H. Kim and H. Hwang, Appl. Phys. Lett. **74**, 709 (1999).
[575] K. Hess, J. Lee, Z. Chen, J. W. Lyding, Y.-K. Kim, B.-S. Kim, Y.-H. Lee, Y.-W. Kim, and K.-P. Suh, IEEE Trans. Electron Devices **46**, 1914 (1999).
[576] E. Li, E. Rosenbaum, J. Tao, and P. Fang, Proc. IEEE Int. Reliability Phys. Symp., 253 (1999).
[577] C. G. Van de Walle and W. B. Jackson, Appl. Phys. Lett. **69**, 2441 (1996).
[578] E. T. Foley, A. F. Kam, J. W. Lyding, and P. Avouris, Phys. Rev. Lett. **80**, 1336 (1998).
[579] M. Budde, G. Lupke, C. P. Cheney, N. H. Tolk, and L. C. Feldman, Phys. Rev. Lett. **85**, 1452 (2000).
[580] P. J. Chen and R. M. Wallace, J. Appl. Phys. **86**, 2237 (1999).
[581] K. L. Brower and S. M. Meyers, Appl. Phys. Lett. **57**, 162 (1990).
[582] F. W. Smith and G. Ghidini, J. Electrochem. Soc. **129**, 1300 (1982).
[583] J. R. Engstrom, D. J. Bonser, and T. Engel, Surf. Sci. **268**, 238 (1992).
[584] J. M. Gibson and M. Y. Lanzerotti, Nature (London) **340**, 128 (1989).
[585] N. F. Mott, S. Rigo, F. Rochet, and A. M. Stoneham, Philos. Mag. B **60**, 189 (1989).
[586] J. J. Lander and J. Morrison, J. Appl. Phys. **33**, 2089 (1962).
[587] J. Seiple and J. P. Pelz, Phys. Rev. Lett. **73**, 999 (1994).
[588] M. R. Baklanov, V. N. Kruchinin, S. M. Repinsky, and A. A. Shklyaev, React. Solids **7**, 1 (1989).
[589] A. A. Shklyaev and T. Suzuki, Phys. Rev. Lett. **75**, 272 (1995).
[590] A. A. Shklyaev, M. Aono, and T. Suzuki, Phys. Rev. B **54**, 10890 (1996).
[591] H. C. Lu, E. P. Gusev, E. Garfunkel, and T. Gustafsson, Surf. Sci. **351**, 111 (1996).
[592] D. Starodub, E. P. Gusev, E. Garfunkel, and T. Gustafsson, Surf. Rev. Lett. **6**, 45 (1999).
[593] F. J. Himpsel, D. A. Lapiano-Smith, J. F. Morar, and J. Bevk, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface, II*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1993), p. 237.
[594] U. Neuwald, H. E. Hessel, A. Feltz, U. Memmert, and R. J. Behm, Appl. Phys. Lett. **60**, 1307 (1992).
[595] M. Udagawa, M. Niwa, and I. Sumita, Jpn. J. Appl. Phys., Part 1 **33**, 375 (1994).
[596] I. S. Hwang, L. R. Lo, and T. T. Tsong, Surf. Sci. **399**, 173 (1998).
[597] T. Horie, Y. Takakuwa, and N. Miyamoto, Jpn. J. Appl. Phys., Part 1 **33**, 4684 (1994).
[598] H. Kageshima and K. Shiraishi, Phys. Rev. Lett. **81**, 5936 (1998).
[599] M. K. Weldon and Y. J. Chabal, Phys. Rev. Lett. **79**, 2851 (1997).
[600] G. Hollinger, J. F. Morar, F. J. Himpsel, G. Hughes, and J. L. Jordan, Surf. Sci. **168**, 609 (1986).
[601] G. Hollinger, E. Bergignat, H. Chermette, F. Himpsel, D. Lopez, M. Lannoo, and M. Bensoussan, Philos. Mag. B **55**, 735 (1987).
[602] H. Ibach, H. D. Bruchmann, and H. Wagner, Appl. Phys. A: Solids Surf. **29**, 113 (1982).
[603] I. S. Hwang, R. L. Lo, and T. T. Tsong, Phys. Rev. Lett. **78**, 4797 (1997).
[604] Y. J. Chabal, Lucent Technical Memorandum, 1998.
[605] H. Kageshima and M. Tabe, in *Control of Semiconductor Interfaces*, edited by I. Ohdomari, M. Oshima, and A. Hiraki (Elsevier, Amsterdam, 1994), p. 227.
[606] A. A. Shklyaev, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), pp. 277–287.
[607] B. B. Stefanov and K. Raghavachari, Surf. Sci. **389**, L1159 (1997).
[608] V. G. Zavodinsky and I. A. Kuyanov, J. Vac. Sci. Technol. B **15**, 21 (1997).
[609] J. B. Neaton, D. A. Muller, and N. W. Ashcroft, Phys. Rev. Lett. **85**, 1298 (2000).
[610] R. E. Walkup and S. Raider, Appl. Phys. Lett. **53**, 888 (1988).
[611] D. Rioux, F. Stepniak, R. J. Pechman, and J. H. Weaver, Phys. Rev. B **51**, 10981 (1995).
[612] M. Chander, D. A. Goetsch, C. M. Aldao, and J. H. Weaver, Phys. Rev. Lett. **74**, 2014 (1995).
[613] N. Shimizu, Y. Tanishiro, K. Kobayashi, K. Takayanagi, and K. Yagi, Ultramicroscopy **18**, 453 (1985).
[614] J. M. Bermond, J. J. Metois, J. C. Heyraud, and C. Alfonso, Surf. Sci. **331-333**, 855 (1995).
[615] P. Bedrossian and E. Kaxiras, Phys. Rev. Lett. **70**, 2589 (1993).
[616] P. Bedrossian and T. Klitsner, Phys. Rev. B **44**, 13783 (1991).
[617] B. S. Swartzentruber, C. M. Matzke, D. L. Kendall, and J. E. Houston, Surf. Sci. **329**, 83 (1995).
[618] M. Offenberg, M. Liehr, and G. W. Rubloff, J. Vac. Sci. Technol. A **9**, 1058 (1991).
[619] K. E. Johnson and T. Engel, Phys. Rev. Lett. **69**, 339 (1992).
[620] V. D. Borman, O. V. Tapinskaya, V. N. Tronin, and V. I. Troyan, Phys. Low-Dimens. Semicond. Struct. **6**, 7 (1994).
[621] V. D. Borman, O. V. Tapinskaya, V. N. Tronin, and V. I. Troyan, JETP Lett. **60**, 718 (1994).
[622] V. D. Borman, V. I. Troyan, and Y. Y. Lebedinski, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 309.
[623] A. M. Stoneham and C. J. Sofield, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 79.
[624] R. M. C. d. Almeida, S. Goncalves, I. J. R. Baumvol, and F. C. Stedile, Phys. Rev. B **61**, 12992 (2000).
[625] H. Z. Massoud, J. D. Plummer, and E. A. Irene, J. Electrochem. Soc. **132**, 2685 (1985).
[626] S. Dimitrijev and H. B. Harrison, J. Appl. Phys. **80**, 2467 (1996).
[627] M. P. Murrell, C. J. Sofield, and S. Sugden, Philos. Mag. B **63**, 1277 (1991).
[628] F. C. Stedile, I. J. R. Baumvol, J. J. Ganem, S. Rigo, I. Trimaille, G. Battistig, W. H. Schulte, and H. W. Becker, Nucl. Instrum. Methods Phys. Res. B **85**, 248 (1994).
[629] J. J. Ganem, I. Trimaille, P. Andre, S. Rigo, F. C. Stedile, and I. J. R. Baumvol, J. Appl. Phys. **81**, 8109 (1997).
[630] E. P. Gusev, H. C. Lu, T. Gustafsson, and E. Garfunkel, Appl. Surf. Sci. **104/105**, 329 (1996).
[631] E. P. Gusev, H. C. Lu, T. Gustafsson, and E. Garfunkel, Braz. J. Phys. **27**, 302 (1997).
[632] A. Pasquarello, M. S. Hybertsen, and R. Carr, Appl. Phys. Lett. **68**, 625 (1996).
[633] A. Pasquarello, M. S. Hybertsen, and R. Carr, Nature (London) **396**, 58 (1999).
[634] M. Ramamoorthy and S. T. Pantelides, Phys. Rev. Lett. **76**, 267 (1996).
[635] M. Ramamoorthy and S. T. Pantelides, Appl. Phys. Lett. **75**, 1 (1999).
[636] K.-O. Ng and D. Vanderbilt, Phys. Rev. B **59**, 10132 (1999).
[637] D. R. Hamann, Phys. Rev. Lett. **81**, 3447 (1998).
[638] T. Watanabe, H. Fujiwara, H. Noguchi, T. Hoshino, and I. Ohdomari, Jpn. J. Appl. Phys., Part 2 **38**, L366 (1999).
[639] H. Kageshima, K. Shiraishi, and M. Uematsu, Jpn. J. Appl. Phys., Part 2 **38**, L971 (1999).
[640] Y. Tu and J. Tersoff, Phys. Rev. Lett. **84**, 4393 (2000).
[641] W. A. Tiller, J. Electrochem. Soc. **128**, 689 (1981).
[642] S. T. Dunham and J. D. Plummer, J. Appl. Phys. **59**, 2541 (1986).
[643] S. T. Dunham, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1988), p. 477.
[644] B. Leroy, Philos. Mag. B **55**, 159 (1987).
[645] K. Taniguchi, Y. Shibata, and C. Hamaguchi, J. Appl. Phys. **65**, 2723 (1989).

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

[646] T. Tamura, N. Tanaka, M. Tagawa, N. Ohmae, and M. Umeno, Jpn. J. Appl. Phys., Part 1 **32**, 12 (1993).
[647] D. G. Cahill and P. Avouris, Appl. Phys. Lett. **60**, 326 (1992).
[648] S. I. Raider, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface*, edited by C. R. Helms and B. E. Deal (Plenum, New York, 1988), p. 35.
[649] H. Massoud (private communication).
[650] T. Akermark, J. Electrochem. Soc. **147**, 1882 (2000).
[651] R. Pfeffer and M. Ohring, J. Appl. Phys. **52**, 777 (1981).
[652] T. Akermark, L. G. Gosset, J.-J. Ganem, I. Trimaille, and S. Rigo, J. Electrochem. Soc. **146**, 3389 (1999).
[653] M. Hillert, S. Jonsson, and B. Sundman, Z. Metallkd. **83**, 648 (1992).
[654] C. Brosset and I. Idrestedt, Nature (London) **201**, 1211 (1964).
[655] P. Rocabois, C. Chatillon, and C. Bernard, J. Am. Ceram. Soc. **79**, 1361 (1996).
[656] H. Du, R. E. Tressler, and K. E. Spear, J. Electrochem. Soc. **136**, 3210 (1989).
[657] R. V. Giridhar and K. Rose, J. Electrochem. Soc. **135**, 2803 (1988).
[658] P. J. Tobin, Y. Okada, S. A. Ajuria, V. Lakhotia, W. A. Feil, and R. I. Hegde, J. Appl. Phys. **75**, 1811 (1994).
[659] G. Weidner and D. Kruger, Appl. Phys. Lett. **62**, 294 (1993).
[660] R. J. Hussey, T. L. Hoffman, Y. Tao, and M. J. Graham, J. Electrochem. Soc. **143**, 221 (1996).
[661] L. G. Gosset, J. J. Ganem, I. Trimaille, S. Rigo, F. Rochet, G. Dufour, F. Jolly, F. C. Stedile, and I. J. R. Baumvol, Nucl. Instrum. Methods Phys. Res. B **136-138**, 521 (1998).
[662] Y. Okada, P. J. Tobin, and S. A. Ajuria, IEEE Trans. Electron Devices **41**, 1608 (1994).
[663] K.-S. Chang-Liao and H.-C. Lai, Appl. Phys. Lett. **72**, 2280 (1998).
[664] Y. Okada, P. J. Tobein, V. Lakhotia, W. A. Feil, S. A. Ajuria, and R. I. Hegde, Appl. Phys. Lett. **63**, 194 (1993).
[665] R. P. Vasquez and A. Madhukar, Appl. Phys. Lett. **47**, 998 (1985).
[666] L. S. Adam, M. E. Law, K. S. Jones, O. Dokumaci, C. S. Murthy, and S. Hegde, J. Appl. Phys. **87**, 2282 (2000).
[667] E. C. Carr, K. A. Ellis, and R. A. Buhrman, Appl. Phys. Lett. **66**, 1492 (1995).
[668] N. Yasuda, K. Muraoka, M. Koike, and H. Satake, Extended Abstracts in the 19th Int. Conf. Sol. State Devices and Materials, 2001 (to be published Sept. 2001).
[669] M.-Y. Hao, D. Nayak, and R. Rakkhit, IEEE Electron Device Lett. **18**, 215 (1997).
[670] B. Y. Kim, I. M. Liu, H. F. Luan, M. Gardner, J. Fulford, and D. L. Kwong, Tech. Dig. Int. Electron Devices Meet. **1997**, 287.
[671] Z. J. Ma, J. C. Chen, Z. H. Liu, J. T. Crick, Y. C. Cheng, C. Hu, and P. K. Ko, IEEE Electron Device Lett. **15**, 109 (1994).
[672] J. R. Pfiester, F. K. Bake, T. C. Mele, H.-H. Tseng, P. J. Tobin, J. D. Hayden, J. W. Miller, C. D. Gunderson, and L. C. Parrillo, IEEE Trans. Electron Devices **ED-37**, 1842 (1990).
[673] T. Morimoto, H. S. Momose, Y. Ozawa, K. Yamabe, and H. Iwai, Tech. Dig. Int. Electron Devices Meet. **1990**, 429.
[674] T. Aoyama, H. Tashiro, and K. Suzuki, J. Electrochem. Soc. **146**, 1879 (1999).
[675] T. Aoyama, K. Suzuki, H. Tashiro, Y. Tada, and K. Horiuchi, J. Electrochem. Soc. **145**, 689 (1998).
[676] T. Aoyama, K. Suzuki, H. Tashiro, Y. Toda, T. Yamazaki, Y. Arimoto, and T. Ito, J. Electrochem. Soc. **140**, 3624 (1993).
[677] K. A. Ellis and R. A. Buhrman, Appl. Phys. Lett. **74**, 967 (1999).
[678] K. A. Ellis and R. A. Buhrman, J. Electrochem. Soc. **145**, 2068 (1998).
[679] K. Krisch, M. L. Green, F. H. Baumann, D. Brasen, L. C. Feldman, and L. Manchanda, IEEE Trans. Electron Devices **43**, 982 (1996).
[680] H. Hwang, W. Ting, D.-L. Kwong, and J. Lee, Appl. Phys. Lett. **59**, 1581 (1991).
[681] D. Mathiot, A. Straboni, E. Andre, and P. Debenest, J. Appl. Phys. **73**, 8215 (1993).
[682] M. Navi and S. T. Dunham, Appl. Phys. Lett. **72**, 2111 (1998).
[683] R. B. Fair, J. Electrochem. Soc. **144**, 708 (1997).
[684] N. K. Chen and C. Lee, J. Electrochem. Soc. **140**, 2390 (1993).
[685] J. Bustillo, C. Chang, S. Haddad, and A. Wang, Appl. Phys. Lett. **58**, 1872 (1991).
[686] S.-L. Zhang, J.-T. Wang, W. Kaplan, and M. Ostling, Thin Solid Films **213**, 182 (1992).
[687] H. Goto, K. Shibahara, and S. Yokoyama, Appl. Phys. Lett. **68**, 3257 (1996).
[688] J. A. Taylor, G. M. Lancaster, A. Ignatiev, and J. W. Rabalais, J. Chem. Phys. **68**, 1776 (1978).
[689] H. Hwang, W. Ting, B. Maiti, D. L. Kwong, and J. Lee, Appl. Phys. Lett. **57**, 1010 (1990).
[690] H. Fukuda, T. Arakawa, and S. Ohno, Jpn. J. Appl. Phys., Part 2 **29**, L2333 (1990).
[691] K. Kumar, A. I. Chou, C. Lin, P. Choudhury, and J. C. Lee, Appl. Phys. Lett. **70**, 384 (1997).
[692] H. C. Lu, E. P. Gusev, E. Garfunkel, B. W. Busch, T. Gustafsson, T. W. Sorsch, and M. L. Green, J. Appl. Phys. **87**, 1550 (2000).
[693] M. Bhat, D. J. Wristers, L.-K. Han, J. Yan, H. J. Fulford, and D.-L. Kwong, IEEE Trans. Electron Devices **42**, 907 (1995).
[694] S. C. Sun, C. H. Chen, D. L. W. Yen, and C. J. Lin, Tech. Dig. Int. Electron Devices Meet. **1995**, 687.
[695] E. H. Poindexter and W. L. Warren, J. Electrochem. Soc. **142**, 2508 (1995).
[696] K. A. Ellis and R. A. Buhrman, Appl. Phys. Lett. **68**, 1696 (1996).
[697] M. J. Hartig and P. J. Tobin, J. Electrochem. Soc. **143**, 1753 (1996).
[698] T. Y. Chu, W. T. Ting, J. Ahn, and D. L. Kwong, J. Electrochem. Soc. **138**, L13 (1991).
[699] A. Gupta, S. Toby, E. P. Gusev, H. C. Lu, Y. Li, M. L. Green, T. Gustafsson, and E. Garfunkel, Prog. Surf. Sci. **59**, 103 (1998).
[700] M. L. Green, D. Brasen, B. J. Sapjeta, T. W. Sorsch, G. Timp, W. N. Lennard, E. P. Gusev, H. C. Lu, E. Garfunkel, and T. Gustafsson, Proc. Electrochem. Soc. Meeting **98-1**, 745 (1998).
[701] M. L. Green, in *Advances in Rapid Thermal and Integrated Processing*, edited by F. Roozeboom (Kluwer, Dordrecht, 1995), p. 193.
[702] E. P. Gusev, H. C. Lu, E. Garfunkel, T. Gustafsson, M. L. Green, D. Brasen, and E. N. Lennard, J. Appl. Phys. **84**, 2980 (1998).
[703] K. Watanabe and T. Tatsumi, Appl. Phys. Lett. **76**, 2940 (2000).
[704] T. Ito, T. Nozaki, and H. Ishikawa, J. Electrochem. Soc. **127**, 2053 (1980).
[705] F. H. P. M. Habraken, A. E. T. Kuiper, Y. Tamminga, and J. B. Theeten, J. Appl. Phys. **53**, 6996 (1982).
[706] G. A. Ruggles, R. Koba, and R. E. Tressler, J. Electrochem. Soc. **133**, 2549 (1986).
[707] T. Hori, S. Akamatsu, and Y. Odake, IEEE Trans. Electron Devices **39**, 118 (1992).
[708] T. Hori, Microelectron. Eng. **22**, 245 (1993).
[709] S. P. Murarka, C. C. Chang, and A. C. Adams, J. Electrochem. Soc. **126**, 996 (1979).
[710] C. H. F. Peden, Phys. Rev. B **47**, 15622 (1993).
[711] A. A. Saranin, O. L. Tarasova, V. G. Kotljar, E. A. Khramtsova, and V. G. Lifshits, Surf. Sci. **331-333**, 458 (1995).
[712] T. Hori, H. Iwasaki, and K. Tsuji, IEEE Trans. Electron Devices **ED-35**, 904 (1988).
[713] I. J. R. Baumvol, F. C. Stedile, J. J. Ganem, I. Trimaille, and S. Rigo, J. Electrochem. Soc. **143**, 2938 (1996).
[714] T. Nguyen, D. A. Carl, S. V. Nguyen, D. M. Dobuzinsky, and J. W. Korejwa, Appl. Phys. Lett. **63**, 1972 (1993).
[715] H. S. Momose, T. Morimoto, Y. Ozawa, K. Yamabe, and H. Iwai, IEEE Trans. Electron Devices **41**, 546 (1994).
[716] W. L. Hill, E. M. Vogel, V. Misra, P. K. McLarty, and J. J. Wortman, IEEE Trans. Electron Devices **43**, 15 (1996).
[717] H. Fukuda, A. Uchiyama, T. Kuramochi, T. Hayashi, T. Iwabuchi, T. Ono, and T. Takayashiki, Tech. Dig. Int. Electron Devices Meet. **1992**, 465.
[718] M. L. Green, T. Sorsch, L. Feldman, W. N. Lennard, E. P. Gusev, E. Garfunkel, H. C. Lu, and T. Gustafsson, Appl. Phys. Lett. **71**, 2978 (1998).
[719] C. A. PasdeAraujo, Y. P. Huang, and R. Gallegos, J. Electrochem. Soc. **136**, 2035 (1989).
[720] D. E. Kotecki, Semicond. Int. **11**, 109 (1996).
[721] H. Massoud, Microelectron. Eng. **36**, 95 (1997).
[722] K. Ishibashi, B. K. Patnaik, N. R. Parikh, G. S. Sandhu, and P. C. Fazan, J. Vac. Sci. Technol. B **12**, 2822 (1994).
[723] T. P. Ma, Appl. Surf. Sci. **117/118**, 259 (1997).
[724] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[725] K. J. Hubbard and D. G. Schlom, J. Mater. Res. **11**, 2757 (1996).
[726] L. Manchanda, W. H. Lee, J. E. Bower, F. H. Baumann, W. L. Brown, C. J. Case, R. C. Keller, Y. O. Kim, E. J. Laskowski, M. D. Morris, R. L. Opila, P. J. Silverman, T. W. Sorsch, and G. R. Weber, Tech. Dig. Int. Electron Devices Meet. **1998**, 605.
[727] T. M. Klein, D. Niu, W. S. Epling, W. Li, D. M. Maher, C. C. Hobbs, R.

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp

I. Hegde, I. J. R. Baumvol, and G. N. Parsons, Appl. Phys. Lett. **75**, 4001 (1999).
[728] J. Kolodzey, E. A. Chowdhury, T. N. Adam, G. Qui, I. Rau, J. O. Olowolafe, J. S. Suehle, and Y. Chen, IEEE Trans. Electron Devices **47**, 121 (2000).
[729] G. D. Wilk and R. M. Wallace, Appl. Phys. Lett. **74**, 2854 (1999).
[730] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **87**, 484 (2000).
[731] G. D. Wilk and R. M. Wallace, Appl. Phys. Lett. **76**, 112 (2000).
[732] Y. Ma, Y. Ono, L. Stecker, D. R. Evans, and S. T. Hsu, Tech. Dig. Int. Electron Devices Meet. **1999**, 149.
[733] L. Manchanda, M. L. Green, R. B. V. Dover, M. D. Morris, A. Kerber, Y. Hu, J.-P. Han, P. J. Silverman, T. W. Sorsch, G. Weber, V. Donnelly, K. Pelhos, F. Klemens, N. A. Ciampa, A. Kornblit, Y. O. Kim, J. E. Bower, D. Barr, E. Ferry, D. Jacobson, J. Eng, B. Busch, and H. Schulte, in *Si-Doped Aluminates for High Temperature Metal Gate CMOS: Zr-Al-Si-O, A Novel Gate Dielectric for Low Power Applications* (IEEE, San Francisco, 2000), pp. 23–26.
[734] R. A. McKee, F. J. Walker, and M. F. Chisholm, Phys. Rev. Lett. **81**, 3014 (1998).
[735] B. Cheng, M. Cao, R. Rao, A. Inani, P. VandeVorde, W. M. Greene, J. M. C. Stork, Z. Yu, P. M. Zeitzoff, and J. C. S. Woo, IEEE Trans. Electron Devices **46**, 1537 (1999).
[736] D. J. Frank, Y. Taur, and H. S. P. Wong, IEEE Electron Device Lett. **19**, 385 (1998).
[737] R. N. Sharma and A. C. Rastogi, J. Appl. Phys. **74**, 6691 (1993).
[738] M. A. Cameron and S. M. George, Thin Solid Films **348**, 90 (1999).
[739] M. Ritala, M. Leskela, J.-P. Dekker, C. Mutsaers, P. J. Soininen, and J. Skarp, Chem. Vap. Deposition **5**, 7 (1999).
[740] A. Chatterjee, R. A. Chapman, K. Joyner, M. Otobe, S. Hattangady, M. Bevan, G. A. Brown, H. Yang, Q. He, D. Rogers, S. J. Fang, R. Kraft, A. L. P. Rotndaro, M. Terry, K. Brennan, S.-W. Aur, J. C. Hu, H.-L. Tsai, P. Jones, G. Wolk, M. Aoki, M. Rodder, and I.-C. Chen, Tech. Dig. Int. Electron Devices Meet. **1998**, 777.
[741] A. Yagishita, T. Saito, K. Nakajima, S. Inumiya, Y. Akasaka, Y. Ozawa, K. Hieda, Y. Tsunashima, K. Suguro, T. Arikado, and K. Okumura, IEEE Trans. Electron Devices **47**, 1028 (2000).
[742] Y. Kim, S. M. Lee, C. S. Park, S. I. Lee, and M. Y. Lee, Appl. Phys. Lett. **71**, 3604 (1997).
[743] F. Rochet, H. Roulet, G. Dufour, S. Carniato, C. Guillot, N. Barrett, and M. Froment, Appl. Surf. Sci. **59**, 117 (1992).
[744] H.-S. Tao, E. P. Gusev, H. C. Lu, E. Garfunkel, T. E. Madey, J. Rowe, and M. L. Green (unpublished).
[745] Z. H. Lu, R. J. Hussey, M. J. Graham, R. Cao, and S. P. Tay, J. Vac. Sci. Technol. B **14**, 2882 (1996).
[746] S. R. Kaluri and D. W. Hess, Appl. Phys. Lett. **69**, 1053 (1996).
[747] A. B. Gurevich, M. K. Weldon, Y. J. Chabal, R. L. Opila, and J. Sapjeta, Appl. Phys. Lett. **74**, 1257 (1999).
[748] G. M. Rignanese, A. Pasquarello, J. C. Charlier, X. Gonze, and R. Car, Phys. Rev. Lett. **79**, 5174 (1997).
[749] A. Ourmazd, D. W. Taylor, J. A. Rentschler, and J. Bevk, Phys. Rev. Lett. **59**, 213 (1987).
[750] J. H. Stathis and D. J. DiMaria, in *Defect Generation and Reliability of Ultra-thin SiO2 at Low Voltage* (Electrochemical Society Toronto, 2000), pp. 33–44.

Downloaded 18 Feb 2002 to 128.6.54.49. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/japo/japcr.jsp